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## SYSTEM APPLICATIONS GUIDE

## SECTION 8

### AUDIO APPLICATIONS

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#### AUDIO PREAMPLIFIERS, LINE DRIVERS, AND LINE RECEIVERS

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#### AUDIO PREAMPLIFIERS

8

Audio signal preamplifiers (preamps) represent the low-level end of the dynamic range of practical audio circuits using modern IC devices. In general, amplifying stages with input signal levels of 10 mV or less fall into the preamp category. This section discusses some basic types of audio preamps, which are:

■ *Microphone* - including preamps for dynamic, electret and phantom powered microphones, using both transformer and transformerless circuits operating from dual and single supplies.

■ *Phonograph* - including preamps for moving magnet and moving coil phono cartridges using a variety of topologies, with detailed frequency response analysis and discussion.

■ *Tape* - including preamp designs useful for a wide range of playback standards including NAB and IEC, covering various time constants/tape speeds.

In general, when working signals drop to a level of 1 mV, the input noise generated by the first system amplifying

stage becomes important for wide dynamic range and good signal-to-noise ratio. For example, if the internally generated noise voltage of an input stage is 1  $\mu$ V and the input signal voltage 1 mV, the very best signal-to-noise ratio possible is just 60 dB.

In a given application, both the input voltage level and impedance of a source are usually fixed. Thus, for best signal-to-noise ratio, the input noise generated by the first amplifying stage must be minimized when operated from the intended source. This factor has definite implications to the preamp designer, as a "low noise" circuit for low impedances is quite different from one with low noise operating from a high impedance.

Successfully minimizing the input noise of an amplifier requires a full understanding of all the various factors which contribute to total noise. This includes the amplifier itself as well as the external circuit in which it is used, in fact *the total circuit environment must be considered*, both to minimize noise and to maximize dynamic range and general signal fidelity.

A further design complication is the fact that not only is a basic gain or signal scaling function to be accomplished, but *signal frequency response* may also need to be altered in a predictable manner. Microphone preamps are an example of

wideband, flat frequency response, low noise amplifiers. In contrast, preamps for phonograph and tape circuits not only scale the signal, they also impart a specific frequency response characteristic to it.

## MICROPHONE PREAMPLIFIERS

The microphone preamplifier (mic preamp) is a basic low level audio amplification requirement. Mic preamps can assume a variety of forms, considering the wide range of possible signal levels, the microphone types, and their impedances. These factors influence the

optimum circuit for a specific application. In this section mic preamps are discussed which work with both high and low impedance microphones, both with and without phantom power, and with transformer as well as transformerless input stages.

### Single-Ended, Single-Supply High-Impedance Mic Preamp

A very simple form of mic preamp is shown in Figure 8.1. This is a non-inverting stage with a single-ended input, most useful with high-impedance microphones such as dynamic and

piezoelectric types. As shown it has an adjustable gain of 20-40 dB via variable resistance  $R_{GAIN}$ , and is useful with microphones (or other sources) with impedances of 600 $\Omega$  or more.

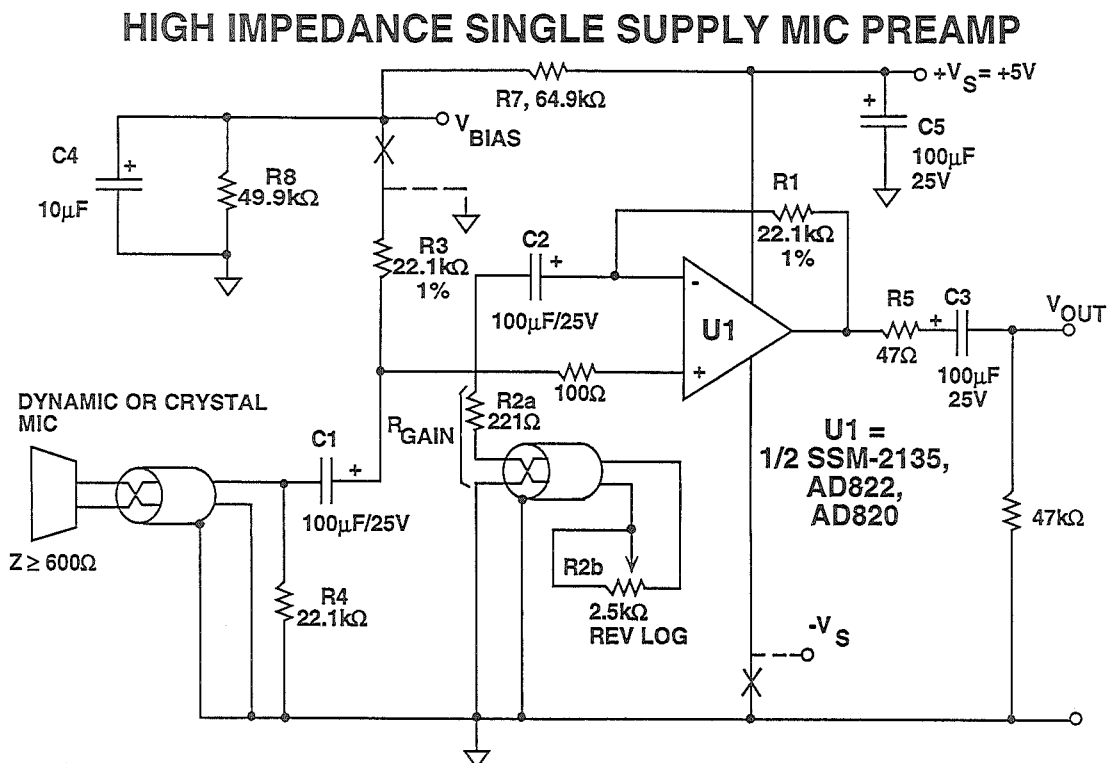


Figure 8.1



The op amp used for U1 greatly affects the overall performance, both in general amplification terms but also in suitability for single supply operation, as shown here. In terms of noise performance, U1 should have a low input noise with  $\geq 500\Omega$  sources, with the external circuit values adjusted so that the source impedance (microphone) dominates the overall source resistance. For very low noise on a single 5V power supply, very few devices are suitable. Among these the dual SSM-2135 and AD822 as well as the single AD820 stand out, and are recommended as first choices. Many other low noise devices can work well in this circuit when the total supply voltage is 10V or more, for example the OP-275, and OP-270/470 types. The circuit can also be easily adapted for dual supply use, as noted below.

In this circuit, gain-determining resistors  $R_1 \parallel R_2$  (where  $R_{2a} + R_{2b} = R_{\text{GAIN}}$ ) are scaled such that their total resistance is less than the expected source impedance, that is  $1k\Omega$  or less. This minimizes the contribution of the gain resistors to input noise at high gain. As noted, gain of the circuit is adjusted in the feedback path via resistor  $R_{\text{GAIN}}$ . Control of a microphone or other low level channel signal level is preferably done after it has been amplified, as here.

Because of single supply operation, input and output coupling is of necessity via capacitors, three in the circuit itself and 2 more for bypassing. These should preferably be low ESR types (which is a byproduct of the higher voltage rating).

For lowest noise in the surrounding circuit, the amplifier biasing must also be *noiseless*, that is free from noise added directly or indirectly by the

biasing.<sup>[1]</sup> Resistors with DC across them should have low excess noise, or be AC-bypassed. Thus  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_7$ , and  $R_8$  are preferably metal films, and  $R_7$ - $R_8$  are bypassed. A 2.2V bias source is provided from  $R_7$ - $R_8$ , which biases the output of U1 about mid-supply. If higher supply voltages are used,  $R_7$ - $R_8$  can be adjusted for maximum output swing for a particular amplifier.

While the SSM-2135 is optimum for U1 when operating from low impedance sources, the FET input AD820 (or AD822) is preferable when using high impedance sources, such as crystal or ceramic mics. To adapt the circuit for such sources,  $R_3$  and  $R_4$  should be  $1M\Omega$  or more, and  $C_1$  can be a  $0.1\mu\text{F}$  film capacitor.

Bandwidth is about  $30k\text{Hz}$  at maximum gain using the SSM-2135, or about  $20k\text{Hz}$  for similar conditions with the AD822 (or AD820). Distortion and noise performance will reflect the device chosen for U1 and the source impedance. With a shorted input, the SSM-2135 has an output noise of about  $110\mu\text{V}_{\text{rms}}$  at a gain of 100, with a  $1k\text{Hz}$  THD+N of 0.022% at  $1\text{V}_{\text{rms}}$  into a  $2k\Omega$  load. The AD820 measures about  $200\mu\text{V}_{\text{rms}}$  with 0.05% THD+N under similar conditions. For either device, these figures will improve at lower gains.

The circuit of Figure 8.1 is good if modest performance and simplicity are required, but will require attention to details for best results. The input cable to the microphone must be shielded, and should be no longer than required. Similar comments apply to any cable used for  $R_{\text{GAIN}}$ . To adapt the circuit for dual supply use,  $R_3$  is returned to ground, and U1 is operated on symmetric supplies ( $\pm V_s = \pm 5\text{V}$ ,  $\pm 15\text{V}$ , etc.)

Although microphones with impedances of less than  $600\Omega$  can be used with this circuit, noise performance will not be optimum, and many such microphones also require a balanced input interface.

## Electret Mic Interface

A popular microphone for speech recording and other non-critical applications is the electret. This is a polarized condenser microphone, typically with a built in FET amplifier. The amplified output signal is taken from the same lead which supplies the microphone with DC power, typically from a 5-10V DC source.

Figure 8.2 illustrates an interface circuit which is useful in powering and scaling the output signal of an electret mic for further use. In this case the

Circuits which show methods of optimizing noise performance with low impedance, balanced output microphones are illustrated below.

scaled output signal from this interface is fed into the LEFT and RIGHT inputs of an AD1848 or AD1849 16 bit CODEC for digitization and processing. DC phantom power is fed to the two mic capsules by the  $R_A$ - $C_A$ - $R_B$  decoupling network from the +5V supply, and the AC output signal is tapped off by  $C_{IN}$ - $R_2$ , and fed into a scaling amplifier, U1. The  $R_B$  resistors may of course vary with different electret mics and DC supply voltages, and the values shown are typical.

## ELECTRET MIC INTERFACE FOR AD1848 OR AD1849 CODEC

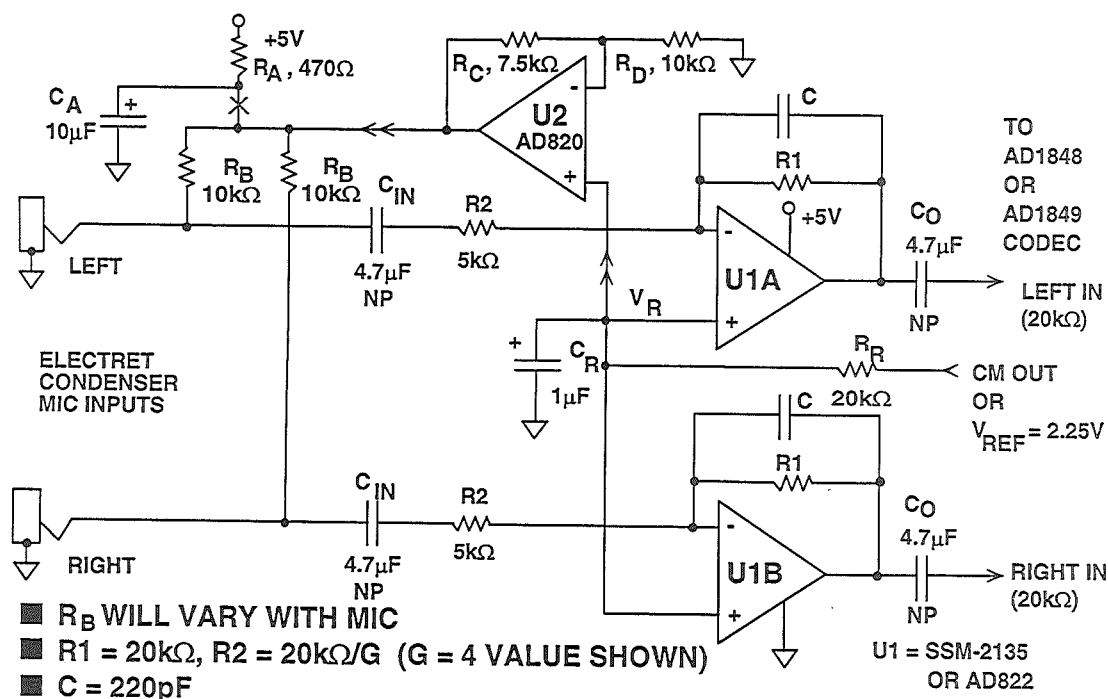


Figure 8.2

The U1 scaling amplifier is a dual SSM-2135 or AD822, and is used here to normalize the mic signal to either a 1Vrms line level or 100mVrms mic level required by the CODEC inputs, and also to low pass filter it prior to digitization. With a wide variety of electret mics and operating parameters, some scaling or normalization of signal level is often required.

Here the scaling gain is simply  $R_1/R_2$ , and resistor  $R_2$  is selected as noted, to provide the gain "G" so as to yield 1Vrms at the line inputs (or .1Vrms at the mic inputs) of the CODEC, with the rated output from the mic. Note that since the U1 stages are inverting, G can be greater or less than unity. For example, it can be 4, as is shown here, or as required to normalize any practical input signal to an optimum level for the CODEC. The amplifier's low pass corner frequency is set by the time constant  $R_1 \cdot C$ , resulting in a -3dB point of 36kHz. DC bias for the two U1 stages is

provided from the CODEC, via the  $V_{REF}$  or CMOUT pins, which provides a filtered 2.25V reference voltage.

The low frequency time constants  $C_{IN} \cdot R_B/R_2$  and  $C_O \cdot 20k\Omega$  are wideband, to minimize LF phase shift. For speech or other narrowband uses, these (non-polar) capacitors can be reduced to 1 $\mu$ F or less.

If a more stable and quiet supply voltage for mics than the system 5V supply is desired, a filtered and scaled version of  $V_R$  can be generated by the optional U2 connected as shown. The output from U2, rather than the output voltage from  $R_A \cdot C_A$ , feeds the two  $R_B$ s directly. When an AD820 is used for U2, resistors  $R_C \cdot R_D$  scale  $V_R$  up to 4V for the values shown. Note that if output voltages within 1V of the 5V supply are required, the U2 op amp must be a rail-rail device, such as an AD820 or AD822.

### Transformer-Coupled Low-Impedance Mic Preamps

For any op amp, the best noise performance is attained when the characteristic *noise resistance* of the amplifier,  $R_n$ , is equal to the source resistance,  $R_s$ . Examples of microphone preamps that make use of this factor are discussed in this section. They utilize an input matching transformer to optimize an amplifier to a source impedance which is not equal to the amplifier  $R_n$ .

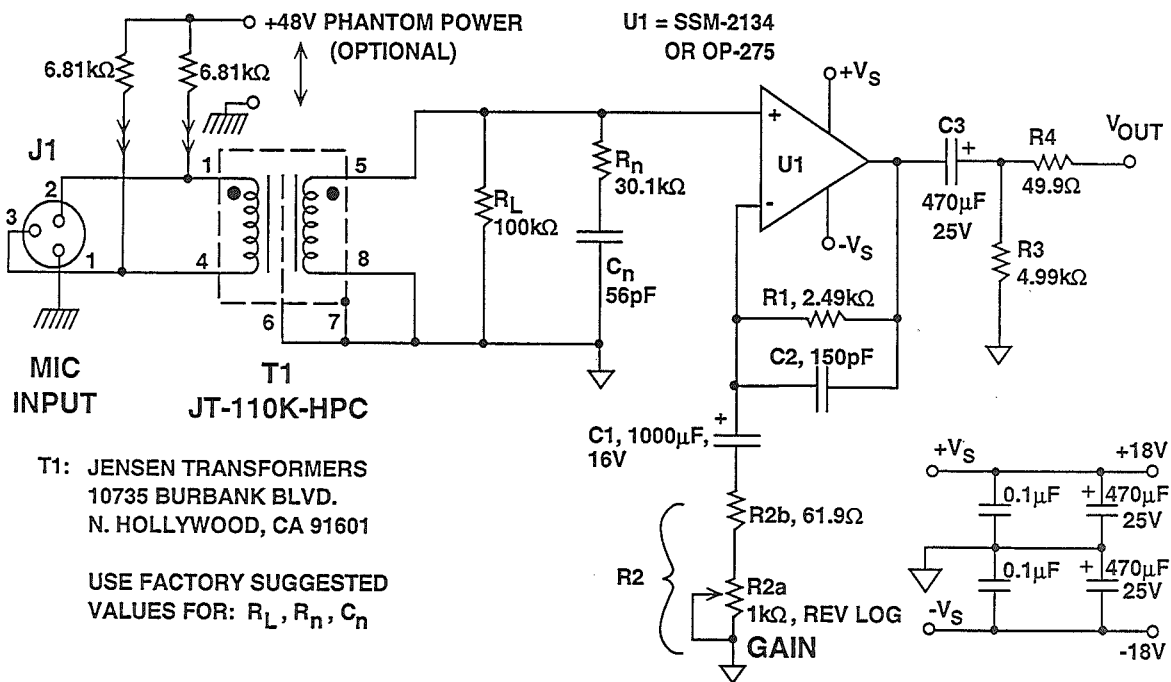
A basic circuit operating on this principle is shown in Figure 8.3. In order to

select an optimum transformer turns ratio to match a given source resistance ( $R_s$ ) to the characteristic  $R_n$  of the op amp in use,  $R_n$  must first be calculated from data for  $e_n$  and  $i_n$  as follows:

$$R_n = \frac{e_n}{i_n} \quad \text{Eq. 8.1}$$

where  $e_n$  is in V/ $\sqrt{\text{Hz}}$  and  $i_n$  is in A/ $\sqrt{\text{Hz}}$ .

## TRANSFORMER INPUT MIC PREAMP WITH 28 TO 50dB GAIN



### Figure 8.3

Then, a turns ratio for T1 may be calculated as:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}} \quad \text{Eq. 8.2}$$

where  $N_s/N_p$  is the transformer secondary/primary turns ratio. For the SSM-2134 amp, the values of  $e_n$  and  $i_n$  are  $3.5\text{ nV}/\sqrt{\text{Hz}}$  and  $0.6\text{ pA}/\sqrt{\text{Hz}}$ , respectively; thus,

$$R_n = \frac{e_n}{i_n} = \frac{3.5 \times 10^{-9}}{0.6 \times 10^{-12}} = 5.8 \text{ k}\Omega$$

Since both  $e_n$  and  $i_n$  vary with frequency,  $R_n$  will also vary with frequency. Therefore, a value calculated for  $R_n$  from the data sheet (such as above) is most accurate at the specified frequency. If the amplifier is to be optimized for a specific frequency, then the  $e_n$  and  $i_n$  values should be for that frequency. However audio amplifiers are wideband circuits, so some compromise is likely. When available, a minimum-noise-figure plot for the amplifier will allow graphical determination of the optimum source resistance for least noise.

For this case, an optimum transformer turns ratio can be calculated to provide the optimum  $R_n$  to the op amp, working from a given  $R_s$ . For example, if  $R_s$  is  $150\Omega$ , then an optimum turns ratio for an SSM-2134 (or other amplifier) with an  $R_n$  of  $5.8k\Omega$  will be:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}}$$

$$= \sqrt{\frac{5.8 \times 10^3}{1.5 \times 10^2}}$$

$$\approx 6.2$$

Other devices with similar  $e_n/i_n$  (and thus  $R_n$ ) can also be so applied, for example the OP-275, the OP-27 or OP-37, and the OP-270/470 types, etc.

Since transformers are catalogued and stocked in fairly narrow and specific impedance ranges, a unit with a rated secondary impedance in the range of 5k $\Omega$  to 10k $\Omega$  will be useful (since the amplifier minimum noise impedance is reasonably broad). Suitable units for this purpose are the Jensen JT-13K7-A, JT-110K-HPC, and the JT-115K-E. Of course, T1 must be adequately shielded and otherwise suitable for operation in low-level environments.

The use of a matching transformer allows the circuit to achieve an equivalent input noise (referred to the transformer input) that is only a few decibels above the theoretical limit, or very close to the thermal noise of the source resistance. For example, the thermal noise of a 150 $\Omega$  resistor in a 20kHz noise bandwidth at room temperature is 219nV. An actual circuit will have a total input referred noise higher than this ideal, due to the noise-degradation of the transformer plus the op amp.

An additional advantage of the transformer lies in the *effective voltage gain* that it provides, due to the step up turns ratio. For a given circuit total numeric gain,  $G_{total}$ , this reduces the gain required from the op amp U1,  $G(U1)$ , to:

$$G(U1) = \frac{G_{total}}{N_s / N_p} \quad \text{Eq. 8.3}$$

Thus, in the composite circuit of Figure 8.3 gain  $G_{total}$  is the product of the transformer step up,  $N_s/N_p$ , and  $(R_1 + R_2)/R_1$ , which is  $G(U1)$ . This has advantages of allowing more amplifier loop gain, thus greater bandwidth and accuracy, lower distortion, etc.

The transformer input mic preamp stage of Figure 8.3 uses the JT-110K-HPC transformer for T1 with a primary/secondary ratio of about 1/8 (150 $\Omega$ /10k $\Omega$ ). The op amp section has a variable gain of about 3.3-41 times, which, in combination with the 17.8dB transformer gain, yields a composite gain of 28 to 50 dB (26 to 300 times). Transient response of the composite amplifier (transformer plus U1) is excellent.

The amplifier used as U1 is either a unity gain compensated SSM-2134, or an OP-275 section. U1 operates here on supplies of  $\pm 18V$  (up to  $\pm 22V$  maximum), and can drive 600 $\Omega$ . The power supplies used should be well regulated and decoupled close to U1, particularly when low impedance loads are driven.

For best results, passive components should be high-quality, such as 1% metal film resistors, a reverse log taper film pot for  $R_{2a}$ , and low ESR capacitors for  $C_1$  &  $C_3$ . Microphone phantom powering<sup>[2,3]</sup> can be used, simply by adding the  $\pm 0.1\%$  matched 6.81k $\Omega$  resistors and a 48V DC source, as shown. Close matching of the DC feed resistors is recommended by the transformer manufacturer whenever phantom power is used, to optimize CMR and to minimize the transformer's primary DC current flow.<sup>[4]</sup> Note that use of phantom powering has little or no effect on the preamp, since the

transformer decouples the CM DC variations at the primary. CMR in an input transformer such as the JT-110K-HPC is typically 85dB or more at 1kHz, and substantially better at lower frequencies. Lower impedance ratio types such as the JT-16A (below) have even higher typical 1kHz CMR, i.e. 100dB.

Performance of this mic preamp for THD+N is shown in the family of curves in Figures 8.4 and 8.5, reflecting use of

the OP-275 and SSM-2134 devices, respectively. The test conditions are 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into 600Ω. For these distortion tests as well as most of those following throughout these sections, THD+N frequency sweeps at various levels are used for sensitivity to slewing related distortions<sup>[5-7]</sup>, while output loaded tests are used for sensitivity to load related non-linearities.

**TRANSFORMER INPUT MIC PREAMP WITH OP-275**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 0.5, 1, 2, \text{ AND } 5V \text{ rms}$ , GAIN = 35dB,  $R_L = 600\Omega$**

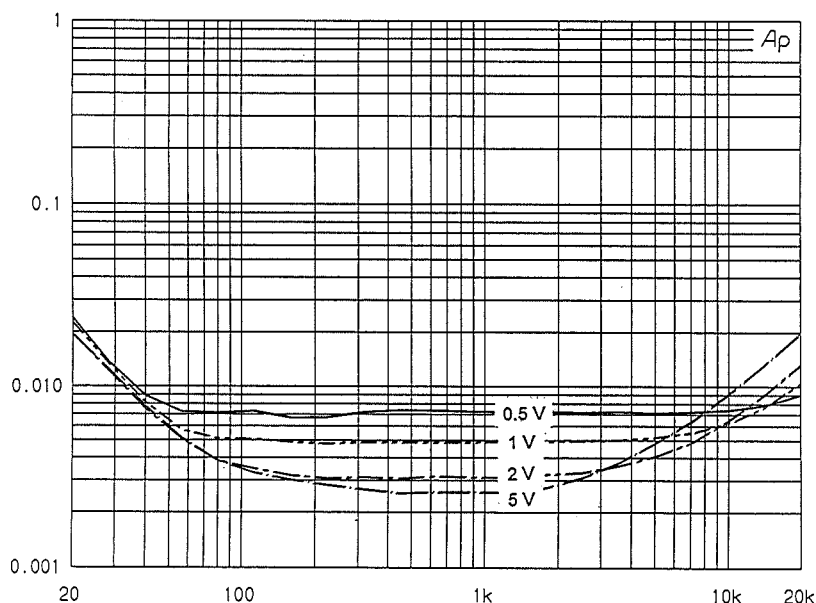
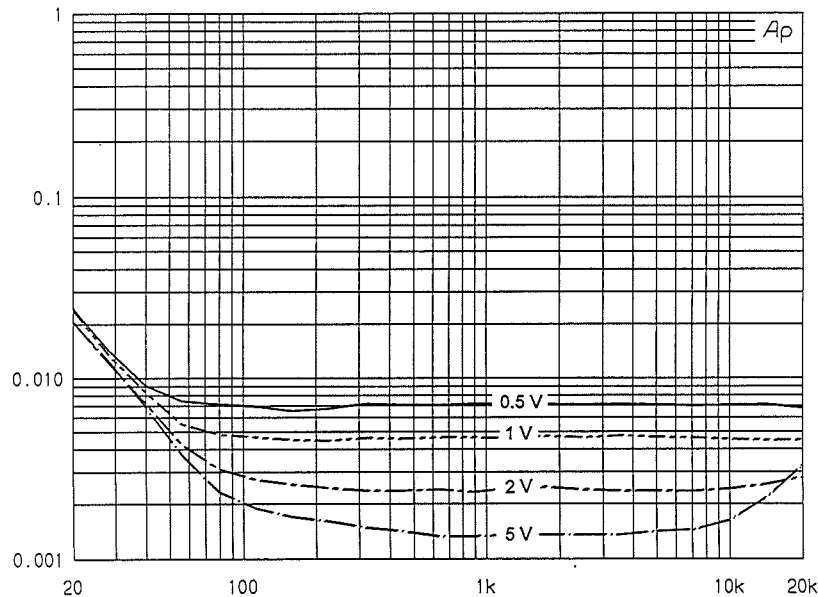


Figure 8.4

**TRANSFORMER INPUT MIC PREAMP WITH SSM-2134**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 0.5, 1, 2, \text{ AND } 5V \text{ rms}$ ,  $GAIN = 35dB$ ,  $R_L = 600\Omega$**



**Figure 8.5**

For the OP-275, as shown in Figure 8.4, there exist three regions of interest, a low frequency region below 100Hz where distortion is largely due to the transformer, a mid-band region from 100Hz-3kHz where distortion is lowest, and the region above 3kHz where the distortion rises. Over most of the frequency spectrum THD+N is 0.01% or less for medium output levels, becoming slightly higher at high frequencies. For the SSM-2134 performance shown in Figure 8.5 there is the same rise at low frequencies due to the transformer, but THD+N is below 0.01% at all frequencies above 50Hz, and at all levels.

The -3dB bandwidth of this circuit is about 100kHz, and is dominated by the JT-110K-HPC transformer and its termination network, assuming a 150 $\Omega$  source impedance. Conversely, for higher or lower source impedances, the bandwidth will lower or rise in propor-

tion, so applications of this circuit should take this into account. Some provision should be made to control the source impedance with a build-out pad prior to the transformer, if it is to be used with source impedances lower than 150 $\Omega$ .<sup>[4]</sup> One such example is capacitor microphone capsules with emitter follower outputs, which appear as a  $\approx 15\Omega$  source.

A circuit functioning similarly to Figure 8.3 but with servo control of offset could also be an option, by using a second op amp as a servo amp. Alternately, the mic preamp in Figure 8.6 shows an optimized servo stage used for this purpose, which allows elimination of capacitors  $C_1/C_3$  and direct coupling to the load.

Finally, although this transformer input preamp has been discussed in terms of a low impedance source

(microphone), the transformer-matching technique is applicable to other transducers of any impedance. It is only necessary to know the characteristic noise resistance of the op amp. If this data is not given in terms of  $e_n$  and  $i_n$ , it is usually implicit from the curves of noise figure versus source resistance.

The noise figure is at a minimum when  $R_n = R_s$ ; therefore, it is only necessary to verify the source resistance for minimum noise figure, which will be very close to  $R_n$ . This resistance can then be used in the transformer selection process.

### Very Low Noise Transformer Coupled Mic Preamps

A high performance low noise mic preamp is shown in Figure 8.6, using a lower ratio transformer, the Jensen JT-16A. This transformer has a lower nominal step up ratio, about 2/1, and is optimized for use with lower noise

resistance amplifiers such as the AD797. The general topology is similar to the previous transformer coupled preamp, but detailed differences allow for higher levels of performance.

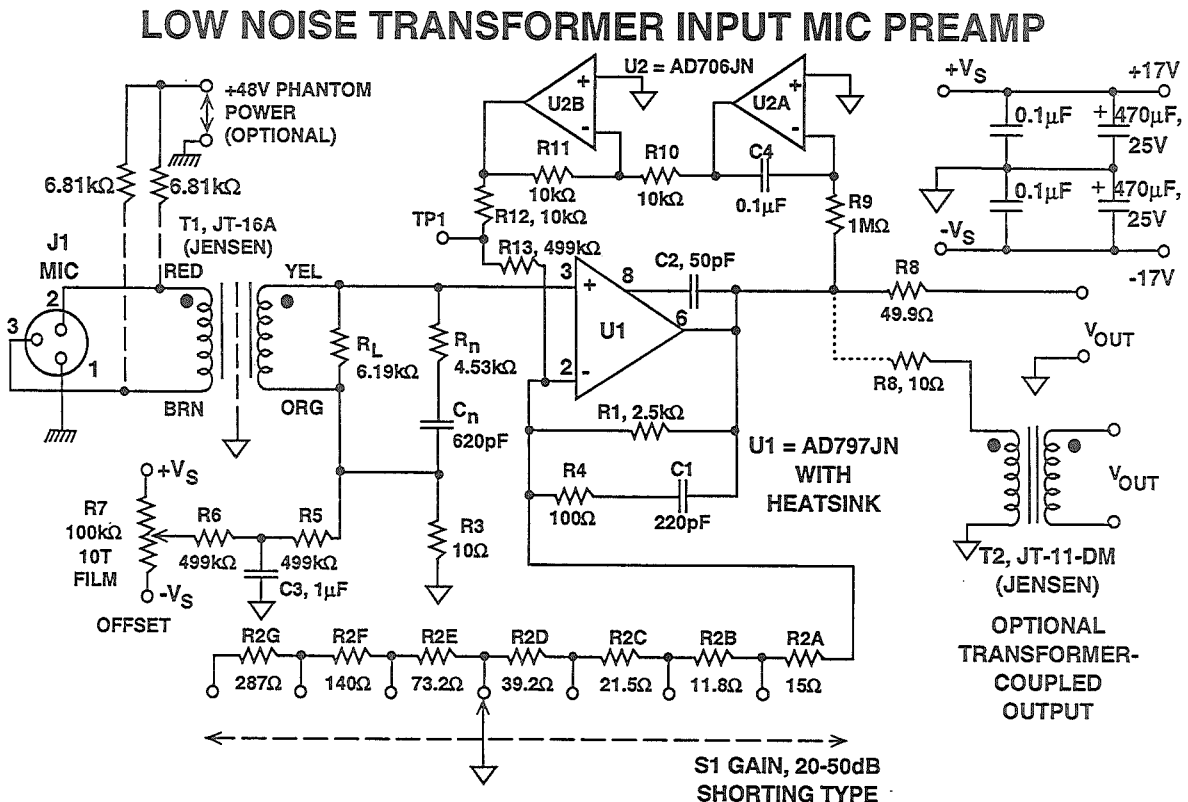


Figure 8.6

This preamp has switch selected variable gain, using switch S1 to alter  $R_2$  of the feedback network to vary U1's gain (and thus overall gain) according to

Figure 8.7. The range chosen is 20-50dB, suitable for a wide range of uses, and gain is selected in 5dB increments.



## R2 VALUES FOR 20 TO 50 dB GAINS

TOTAL GAIN, dB	U1 GAIN, dB	R2 (TOTAL), $\Omega$	"R2N", $\Omega$
50	44.4	15.15	15.0
45	39.4	27.07	11.8
40	34.4	48.56	21.5
35	29.4	87.68	39.2
30	24.4	160.3	73.2
25	19.4	300	140
20	14.4	588.5	287

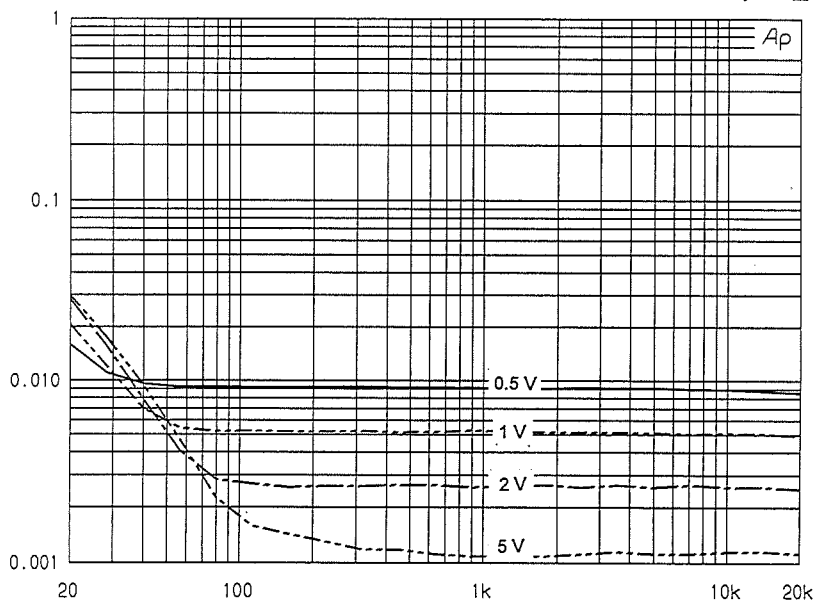
- T1 Provides a Fixed 5.6dB Gain
- R2N is individual R2A, R2B, etc.
- Closest Standard Values are Shown

Figure 8.7

Inasmuch as the AD797 has high DC precision as well as low distortion audio characteristics, this circuit can be DC coupled quite effectively. Initial device offset of the AD797 is  $80\mu\text{V}(\text{max})$ , allowing a simple trim by  $R_7$  to null output offset. Offset is trimmed out with the servo temporarily defeated by grounding test point TP1, and trimming the output DC to less than 1mV, while at a mid-range gain setting of 35dB. Offset shift with gain is only a few mV, and is of little concern, as the servo circuit composed of U2A and U2B holds longer term DC offset to  $100\mu\text{V}$  or less, with very little gain interaction.

Performance of this mic preamp for THD+N is shown in Figure 8.8, for conditions of 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into  $600\Omega$ . From these data it is clear that essentially the only distortion in the circuit is due to the transformer, and this is quite small and only present at the lowest frequencies. Above 100Hz, the apparent distortion is noise limited, continuing through to the highest frequencies.

**LOW NOISE TRANSFORMER INPUT MIC PREAMP**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 0.5, 1, 2, \text{ AND } 5\text{ V rms}$ , GAIN = 35dB,  $R_L = 600\Omega$**



**Figure 8.8**

The -3dB bandwidth of this circuit is just under 150kHz, and while essentially dominated by the JT-16A transformer and termination, reduces slightly at the highest gain (50dB). Like the previous transformer coupled circuit, this circuit also assumes a 150Ω source impedance, and similar caveats in application are true. Reference [4] includes information on both build out and fixed loss input pads, and other practical interfacing considerations for transformers.

The basic circuit as shown is single-ended with  $V_{OUT}$  taken from  $R_8$ , but a

transformer can be added to drive balanced lines. If used, T2 is a JT-11-DM (or similar) nickel core type for lowest distortion, and is coupled to U1 as shown.

If very high levels of output drive are necessary or long lines are to be driven, a dedicated high current output driver should be used with U1, as described in the “Line Drivers” section. This can be most easily implemented by making U1 a composite amplifier employing an AD797 input section plus a unity-gain follower output stage, using the AD811.

## Transformerless Input Low-Impedance Mic Preamp

Another method of amplifying low level balanced mic signals is the use of a *transformerless* differential input stage, using an instrumentation amplifier (in-amp) as the preamp. The in-amp (in IC or other form) is configured for gain with just one resistor. It provides transformerless gain with good rejection of CM noises such as hum, and has low operating noise with commonly used mics.

Figure 8.9 is an example of a low noise transformerless mic preamp, using the SSM-2017P (U1) and an OP- 275GP op amp (U2). This circuit is a mic preamp with gain variable over a range of 6-66dB with an optional phantom power feature.<sup>[8]</sup>

### TRANSFORMERLESS INPUT MIC PREAMP

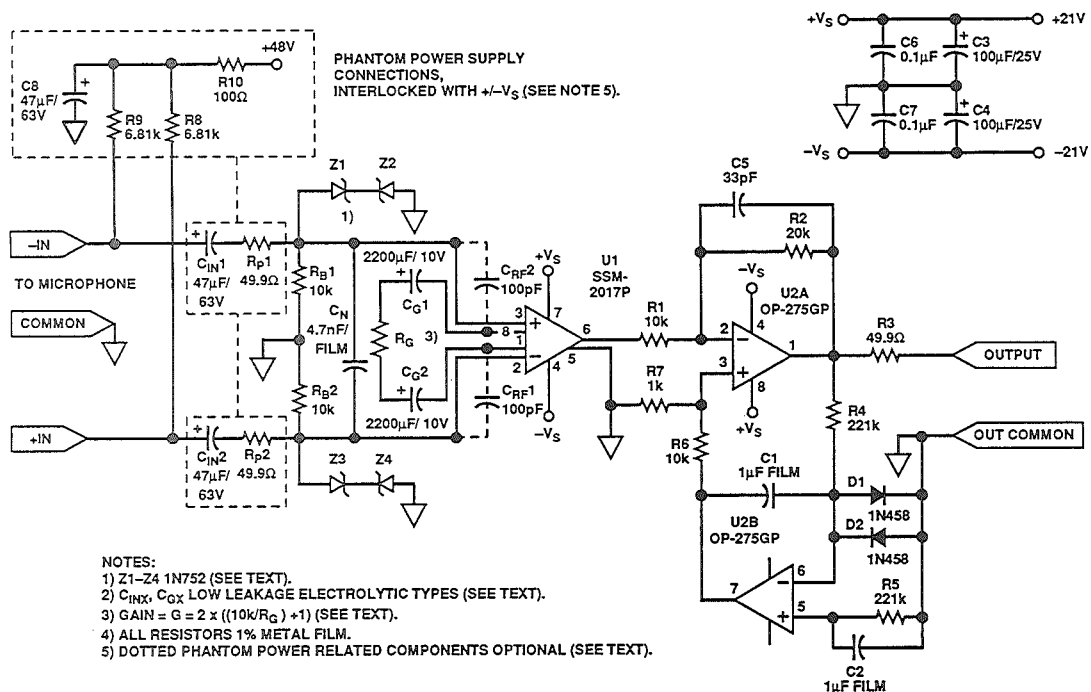


Figure 8.9

The SSM-2017 IC preamp is suitable for use in transformerless mic preamps, with an input noise of less than  $1nV/\text{Hz}$ , high CM rejection and low distortion. Gain of this 8 pin IC is set by one external resistor, " $R_G$ ", and is adjustable over a range of 1-1000 (0 to 60dB). Differential inputs at pins 2-3 allow balanced input signals, with a

single-ended output signal developed between the output (6) and reference (5) pins.

The SSM-2017 is used here in a gain-programmable input stage, which then drives a fixed gain of 2 OP- 275 high current output buffer and DC servo. The buffer provides low distortion drive

into 600Ω loads, with the second half of U2 used as a servo, for low output DC offset (≤ 2mV).

In the U1 stage, gain is set by resistance  $R_g$ . Combined with the gain of two in the U2 stage, the overall preamp numeric gain “G” is:

$$G = 2 \left[ \frac{10,000\Omega}{R_g} + 1 \right] \quad \text{Eq. 8.4}$$

$R_g$  can be either a reverse log pot, or a switch controlled resistance used as a gain control for the entire circuit. The  $R_g$  value for a given gain G is:

$$R_g = \frac{20,000\Omega}{G - 2} \quad \text{Eq. 8.5}$$

Figure 8.10 gives  $R_g$  values for various gains, using the closest standard 1% resistor values.

## GAIN TABLE FOR TRANSFORMERLESS MIC PREAMP

GAIN	GAIN IN dB	$R_g (\Omega) *$
2	6	Open
4	12	10,000
10	20	2,490
20	26	1,100
31.6	30	681
40	32	523
100	40	205
200	46	100
316	50	63.4
400	56	49.9
1000	60	20
2000	66	10

\*  $R_g$  is rounded to closest 1% value

Figure 8.10

Another important requirement for transformerless preamps is that they must be immune to transient damage related to phantom power supplies. With the use of microphone phantom powering, 48V DC power is fed CM to a remote mic capsule, while the balanced audio signal received back from the mic must be amplified cleanly with no side

effects from the DC. For steady state conditions this is simple, but switching transients from the DC power can kill an amplifier input stage if it is not protected. Transformerless mic preamps must be protected against power surges, yet must also operate with best performance.

Normally coupling capacitors  $C_{in1}$  and  $C_{in2}$  decouple the phantom power DC level, passing the balanced audio signal to U1. But, when the phantom power is switched on/off, or the mic cable is plugged in/out, potentially destructive transients of up to  $\pm 48V$  are coupled through  $C_{in1}$  and  $C_{in2}$ , and appear across  $R_{b1}$  and/or  $R_{b2}$ . If these transients are not safely dissipated, they can cause destruction of U1. This applies to *virtually any amplifier input stage, not just the SSM-2017*, since energy stored in the coupling capacitors can develop peak discharge currents of several amperes.

Here CM voltage limiting is used on each of the differential input lines, with pairs of back-to-back low voltage zeners, Z1-Z2 and Z3-Z4, standard 400mW,  $V_z=5.1V$  units from the 1N750 series. Peak current limiting for transient discharge is provided by the protection resistors  $R_{p1}$  and  $R_{p2}$ .

This preamp can be operated with or without phantom power, so it is logical to optimize input connections so that those portions of the circuit not essential for phantom power are not in the signal path and the 48V DC power being switched off when phantom power is not in use. When phantom power is used, the 48V supply should be interlocked with the bipolar power supply of the amplifier to prevent switching on phantom power with the amplifier circuitry off.

Another source of problems with high gain preamps is radio frequency interference (RFI). Input capacitor  $C_n$  filters frequencies above 135kHz before they reach the preamp input. In addition, further filtering is provided in the second stage by  $R_2$ - $C_5$ , at 241kHz.

Additional RFI filtering can use several methods. Separate low resistance inline RF chokes or a single common mode choke can be used in series with the two inputs. RF bypassing of the SSM-2017 input transistors can also be used, from pins 1-2 and 3-8 (shown on the schematic as  $C_{rf1}/C_{rf2}$ ).

This amplifier's performance is quite good over gain ranges of 6-66dB (2/1 to 2000/1). For a typical audio load of 600 $\Omega$ , THD+N at various gains and an output level of 10Vrms is consistent and well below 0.01%, for all but the highest gains, where it becomes more limited by noise, as shown in Figure 8.11. Noise performance is quite good, at an operating gain of 1000 it is equivalent to 1nV/ $\sqrt{Hz}$  referred to the preamp input. Maximum output is a function of the power supplies, and can be as high as 10Vrms. Note that output resistor  $R_3$  limits available swing driving 600 $\Omega$ , but should be retained for short circuit protection. Supply voltages on the order of  $\pm 20V$  are appropriate for highest output into 600 $\Omega$ , but the circuit can also be operated on lower supply voltages with lower maximum output.

# THD + N PERFORMANCE OF TRANSFORMERLESS MIC PREAMP VERSUS GAIN FOR $V_{out} = 10V$ rms, $R_L = 600\Omega$

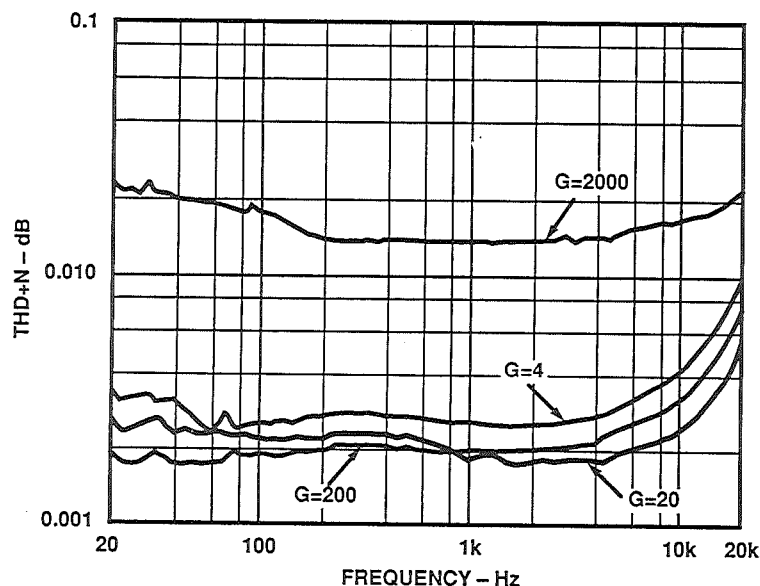


Figure 8.11

The SSM-2017 device architecture is basically similar to family predecessors SSM-2015 and SSM-2016, but without access to the internal gain resistors (because of the 8 pin package). Both the SSM-2015 and SSM-2016 can be applied in circuits similar to Figure 8.9

with phantom powering, and have virtues in their own right. For example, the SSM-2016 can use supplies of up to  $\pm 36V$ , and has a high current output stage ( $\pm 40mA$  minimum). This enables it to drive low impedance audio loads to high levels.

**REFERENCES: MICROPHONE PREAMPLIFIERS**

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## RIAA PHONO PREAMPLIFIERS

An example of an audio range preamplifier application requiring equalized frequency response is the RIAA phono preamp. While present day LP record sales are quickly fading with the establishment of new digital media, for completeness equipment will still be designed to include phono playback stages for some time. RIAA preamp stages, as amplifiers with predictable non-flat frequency response, have more general application connotations. The design techniques within this section

are specific to RIAA as an example, but are applicable to other frequency dependent amplitude designs in general.

The techniques are also useful as a study tool, considering the various approaches which have been advanced to optimize the function of high performance gain with predictable equalization (EQ). These last two points make these discussions useful in a much broader sense.

### RIAA Basics

The RIAA equalization curve<sup>[1]</sup> is shown in Figure 8.12, expressed relative to DC. This curve indicates maximum gain below 50 Hz ( $f_1$ ), with two high-frequency inflection points. Above  $f_1$ , the gain rolls off at 6 dB/octave until a first high-frequency breakpoint is

reached at 500 Hz ( $f_2$ ). Gain then remains relatively constant until a second high-frequency breakpoint is reached at 2.1 kHz ( $f_3$ ), where it again rolls off at 6 dB/octave through the remainder of the audio region and above.

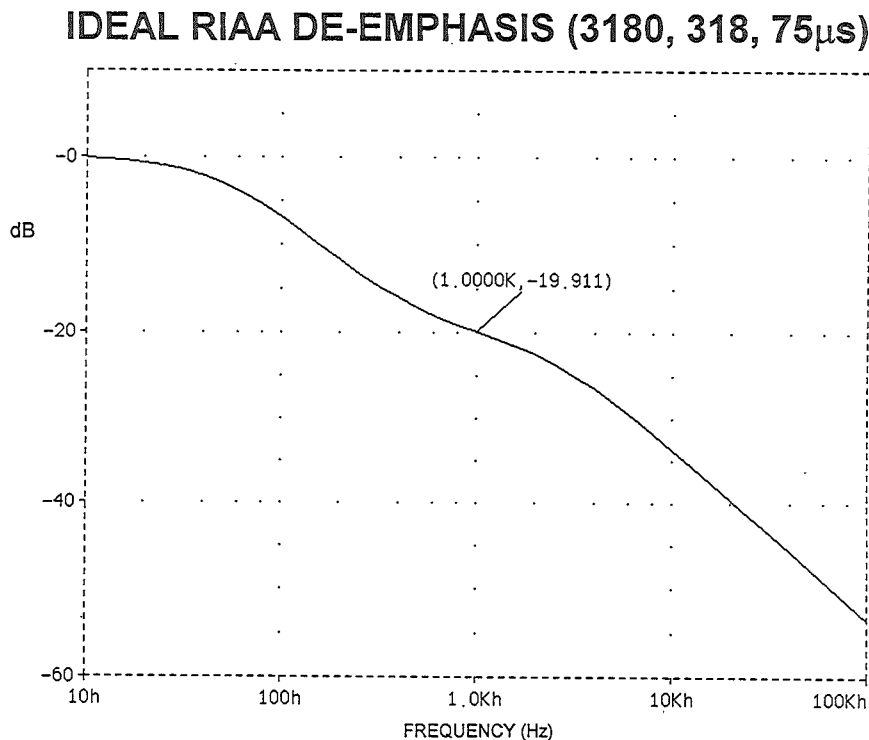


Figure 8.12



Use of a low frequency rolloff ( $f_0$ , not shown) is at the option of the designer. It can be extended towards DC, or, alternately, rolled off at a low frequency below 50 Hz. When applied, this roll off is popularly called a “rumble” filter, since it reduces turntable/record related low-frequency disturbances and lessens the possibility of system and low-frequency driver overload. This rolloff may or may not coincide with a fourth time constant.

However, gain at the frequencies  $f_1$ ,  $f_2$ , and  $f_3$  describes the basic RIAA curve. This curve is also described in terms of three corresponding time constants,  $T_1$ ,  $T_2$ , and  $T_3$ , defined as  $3180\mu\text{s}$ ,  $318\mu\text{s}$ , and  $75\mu\text{s}$ , respectively.<sup>[1]</sup> (Note:  $T_1$ - $T_3$  are here described as they correspond to ascending frequency, or the reverse of the terminology in <sup>[1]</sup>. The time constants themselves are identical, however). An IEC amendment to the basic RIAA response adds a fourth time constant of  $7950\mu\text{s}$ , corresponding to an  $f_0$  of 20Hz when used.<sup>[2]</sup> Use of this rolloff has never been standardized in the US, and is not treated in great detail here.

The characteristic gain in dB for an RIAA preamp is generally specified relative to a 1kHz reference frequency. From Figure 8.13, a complete 10-100kHz relative decibel table for the three basic RIAA time constants, the 1kHz gain is 19.91dB below the DC gain (column 3). Expressed in terms of a gain ratio, this means the ideal 1kHz RIAA preamp gain is 0.101 times the DC gain. This constant 0.101 is unique to all RIAA preamp designs following the above curve, therefore it can be designated as “ $K_{\text{RIAA}}$ ”, or:

$$K_{\text{RIAA}} = 0.101 \quad \text{Eq. 8.6}$$

This constant logically shows up in various gain expressions of the RIAA preamp designs which follow. Since the shape of the standard RIAA curve is fixed, specifying gain for a given frequency (1kHz) defines the gain for all other frequencies. For convenience, Figure 8.13 shows gains relative to 1kHz (column 2), and to DC (column 3).

## IDEALIZED RIAA FREQUENCY RESPONSE

FREQ	VDB(6)(1)	VDB(5)(2)
1.000E+01	1.974E+01	-1.684E-01
1.259E+01	1.965E+01	-2.639E-01
1.585E+01	1.950E+01	-4.109E-01
1.995E+01	1.928E+01	-6.341E-01
2.512E+01	1.895E+01	-9.654E-01
3.162E+01	1.847E+01	-1.443E+00
3.981E+01	1.781E+01	-2.103E+00
5.012E+01	1.694E+01	-2.975E+00
6.310E+01	1.584E+01	-4.067E+00
7.943E+01	1.455E+01	-5.362E+00
1.000E+02	1.309E+01	-6.823E+00
1.259E+02	1.151E+01	-8.398E+00
1.585E+02	9.877E+00	-1.003E+01
1.995E+02	8.236E+00	-1.167E+01
2.512E+02	6.645E+00	-1.327E+01
3.162E+02	5.155E+00	-1.476E+01
3.981E+02	3.810E+00	-1.610E+01
5.012E+02	2.636E+00	-1.727E+01
6.310E+02	1.636E+00	-1.828E+01
7.943E+02	7.763E-01	-1.913E+01
1.000E+03	8.338E-07	-1.991E+01
1.259E+03	-7.682E-01	-2.068E+01
1.585E+03	-1.606E+00	-2.152E+01
1.995E+03	-2.578E+00	-2.249E+01
2.512E+03	-3.726E+00	-2.364E+01
3.162E+03	-5.062E+00	-2.497E+01
3.981E+03	-6.572E+00	-2.648E+01
5.012E+03	-8.227E+00	-2.814E+01
6.310E+03	-9.992E+00	-2.990E+01
7.943E+03	-1.184E+01	-3.175E+01
1.000E+04	-1.373E+01	-3.365E+01
1.259E+04	-1.567E+01	-3.558E+01
1.585E+04	-1.763E+01	-3.754E+01
1.995E+04	-1.960E+01	-3.951E+01
2.512E+04	-2.158E+01	-4.149E+01
3.162E+04	-2.357E+01	-4.348E+01
3.981E+04	-2.557E+01	-4.548E+01
5.012E+04	-2.756E+01	-4.747E+01
6.310E+04	-2.956E+01	-4.947E+01
7.943E+04	-3.156E+01	-5.147E+01
1.000E+05	-3.356E+01	-5.347E+01

Notes:

(1) denotes 1kHz 0dB reference

(2) denotes DC 0dB reference

Figure 8.13

It can also be seen from the RIAA curve of Figure 8.12 that the gain characteristic continues to fall at high frequencies. This implies that an amplifier with unity-gain stability for 100% feedback is required, which can indeed be true, if a standard feedback configuration is

used. There are many circuit approaches which can be used to accomplish RIAA phono-playback equalization, but all must satisfy the general frequency response characteristic of Figure 8.12.

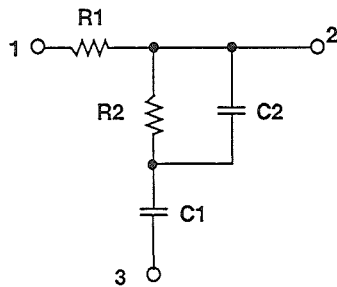
### Equalization Networks for RIAA Equalizers

Two EQ networks well suited in practice to RIAA phono reproduction are illustrated in Figure 8.14a and 8.14b, networks N1 and N2. Both networks with values as listed can yield with high accuracy the three standard RIAA time constants of 3180, 318, and 75 $\mu$ s as outlined by network theory.<sup>[3,4,5,6]</sup>

For convenience, both theoretical values for the ideal individual time constants are shown (left), as well as closest fit standard "no trim" values (right). Designers can of course, parallel and/or series such R and C values as may be deemed appropriate or practical, adhering to network theory.

8

### RIAA NETWORKS ( $T_1 = 3180\mu\text{s}$ , $T_2 = 318\mu\text{s}$ , $T_3 = 75\mu\text{s}$ )



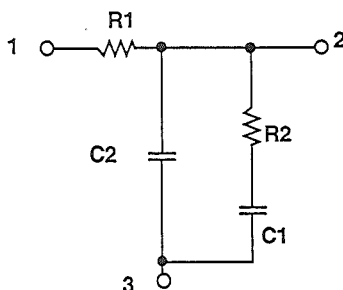
A: "N1" NETWORK

#### THEORETICAL

$R_1 = 9.79\text{k}\Omega$   
 $R_2 = 789.3\Omega$   
 $C_1 = 0.3\mu\text{F}$   
 $C_2 = 0.1029\mu\text{F}$

#### CLOSEST FIT

$R_1 = 9.76\text{k}\Omega$   
 $R_2 = 787\Omega$   
 $C_1 = 0.3\mu\text{F (BASE)}$   
 $C_2 = 0.1\mu\text{F} + 3\text{nF}$



B: "N2" NETWORK

#### THEORETICAL

$R_1 = 7.290\text{k}\Omega$   
 $R_2 = 1.06\text{k}\Omega$   
 $C_1 = 0.3\mu\text{F}$   
 $C_2 = 0.1029\mu\text{F}$

#### CLOSEST FIT

$R_1 = 7.32\text{k}\Omega$   
 $R_2 = 1.05\text{k}\Omega$   
 $C_1 = 0.3\mu\text{F (BASE)}$   
 $C_2 = 0.1\mu\text{F} + 3\text{nF}$

Figure 8.14

Of course there are an infinite set of possible RC combinations from which to choose network values, but practicality should rule any final selection. A theoretical starting point for a network value selection can begin with *any* component, but in practice the much smaller range of available capacitors suggests their selection first, then resistors, from their much broader span of (stock) values. Note that precision film resistors can in fact be obtained (on special order) in virtually *any* value, up to several megohms. The values listed here are those taken as standard from the E96 series.

Very high standards of EQ accuracy are possible, to tolerances of noticeably better than  $\pm 0.1\text{dB}$  (see for example data from [8] also quoted in [6]). In the design process however, there are several distinct general aspects of EQ component selection which can affect the ultimate accuracy. These are worth reviewing before embarking on a design.

■ The *selection tolerance* of the component defines how far an ideal (zero manufacturing tolerance) component deviates from the theoretical value. A good design will seek to minimize this error by using either carefully selected standard values, or series and/or shunt combinations, so as to achieve selection tolerance of less than 1%, preferably zero.

■ The *manufacturing tolerance* of the component defines how far an otherwise ideal component deviates from its stated catalog value, such as  $\pm 1\%$ ,  $\pm 2\%$ , etc. This can obviously be controlled by tighter specifications, but usually at some premium, particularly with capacitors of  $\pm 1\%$  or less. Note that a “hidden” premium here can be long delivery times for certain values. Care should be taken to use standard stock

values with capacitors— even to the extent that multiple standard values may be preferable (3 times  $0.1\mu\text{F}$  for  $0.3\mu\text{F}$ , for example).

■ *Topology-related parasitics* must also be given attention, as they can also potentially wreck accuracy. Amplifier gain-bandwidth is one possible source of parasitic EQ error. However, a more likely error source is the parasitic zero associated with active feedback equalizers. If left uncompensated below  $100\text{kHz}$ , this alone can be a serious error.

In any event, for high equalization accuracy to be “real”, once a basic solid design is selected the designer must provide for the qualification of components used, by precise measurement and screening, or tight purchase tolerances. An alternative is iterative trimming against a reference standard such as [9], but this is not likely to be attractive for production. An example is the data of [8], derived with the network of [9]. If used, the utility of such a trim technique lies in the reduction of the equipment accuracy burden; the comparator used need have high *resolution*, but accuracy is transferred to the network comparison standard used.

It should be understood that an appropriately selected high quality network will yield excellent accuracy, for example either N1 or N2 with the “closest fit” (single component) values of exact value yield a broadband error of about  $\pm 0.15\text{dB}$ . Accuracy about 3 times better than this is achieved with the use of N1 and the composite C<sub>2</sub>, as noted. The composite C<sub>2</sub> is strongly suggested, as without it there is a selection error of about 3%.

It is strongly recommended that only the highest quality components be employed in these networks.

Regardless of the quality of the remainder of the circuit, it is evident that the equalization accuracy and fidelity can be no better than the quality of these components used to define the transfer function. Thus only the best available components should be used in the N1 (or N2) RC network, selected as follows:

■ *Capacitors*— should have close initial tolerance (1-2%), a low dissipation factor and low dielectric absorption, be non-inductive in construction, and have stably terminated low-loss leads. These criteria in general are best met by capacitors of the Teflon, polypropylene and polystyrene film families, with 1-2% polypropylene types being preferred as the most practical.<sup>[10,11,12]</sup> Types which should be avoided are the “high K” ceramic families, while in contrast, “low K” ceramic types, such as “NP0” or “COG” dielectrics, have excellent dissipation factors. While not recommended as readily as the best film types (their DA is not as well controlled as the best films), they may be worth consideration for small values and/or where space is at a premium.

■ *Resistors*— should also be close tolerance ( $\leq 1\%$ ), have low non-linearity (low voltage coefficient), be temperature stable, with solid stable terminations and low-loss non-inductive leads. Types which meet these criteria best are the bulk metal foil types and selected thick films, or selected military grade RN55 or RN60 style metal film resistor types.<sup>[13]</sup>

### RIAA Equalizer Topologies

There are of course many different circuit topologies which can be used to realize an RIAA equalizer, and three possible ones are illustrated in fundamental form in Figures 8.15 through 8.17 of this section. Dependent upon the

The specific component values suggested may not be optimum from a low impedance and low noise standpoint, but the practical realities for general use will most likely deter the use of appreciably lower ones. For example, one could reduce the input resistance of either network to  $1k\Omega$ , and thus lower the input referred noise contribution of the network. But this in turn would necessitate greater drive capability from the amplifier stage, and raise the C values to  $1-3\mu F$ , where they are large, expensive, and very difficult to obtain. This may be justified for some uses, where performance is the guiding criterion rather than cost effectiveness, or the amplifiers used sufficiently low in noise to justify such a step. Regardless of the absolute level of impedance used, the components should be adequately shielded against noise pickup, with the outside foils of  $C_1$  or  $C_2$  connected to common.

These same N1/N2 networks can suffice for both active and passive type equalization. Active (feedback) equalizers use the network simply by returning the input resistor ( $R_1$ ) to common, that is jumpering points 1-3, and employing the network as a two-terminal impedance between points 1+3, and 2. Passive equalizers use the same network in a three terminal mode, interstaged between two wideband gain blocks.

type of phono cartridge to be used, the 1kHz gain of the preamp can range from 30-70dB.

Magnetic phono cartridges in popular use consist of two basic types: moving

magnet and moving coil. The moving magnet types, which are the most familiar, are suitable for the first circuits to be described. The moving coil cartridge types are higher performance devices; they are less commonplace but still highly popular.

Functionally, both types of magnetic cartridges perform similarly, and both must be equalized for flat response in accordance with the RIAA characteristic. A big difference in application, however, is the fact that moving magnet types have typical sensitivities of about 1 mV of output for each cm/s of

recorded velocity. In moving coil types, a sensitivity on the order of 0.1 mV is more common (for a similar velocity). In application then, a moving coil RIAA preamp must have more gain than a moving magnet preamp. Typical overall (1 kHz) gains are 60-70 dB for moving coils and 30-40 dB for moving magnets. Noise performance of a moving coil preamp becomes critical, however, because of low-output voltage and low impedance involved—typically 3-40 ohms. The following circuits illustrate techniques that are useful in meeting these requirements.

### Actively Equalized RIAA Preamp Topology

The most familiar topology is shown in Figure 8.15, and is called an active feedback equalizer, because the network  $N$  used to accomplish the EQ is part of an active feedback path.<sup>[10,14]</sup> In these and the following discussions it

is assumed that the input from the pickup is appropriately terminated by  $R_t$ - $C_t$ , which are selected for flat response. The following discussions deal with the frequency response of the amplifier, given this ideal input signal.

### ACTIVE FEEDBACK RIAA EQUALIZER

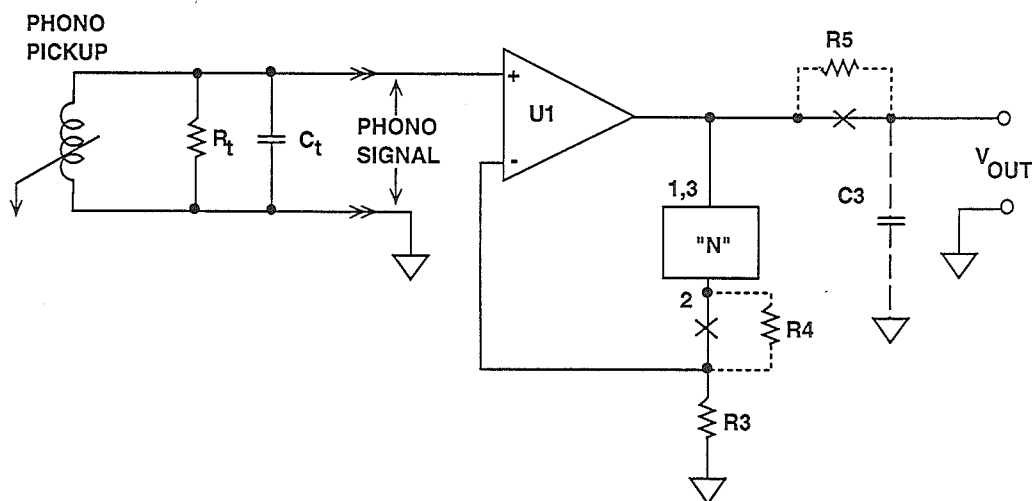


Figure 8.15

Assuming a sufficiently high gain amplifier for U1, the gain/frequency characteristics of this circuit are determined by the network. Gain of the stage is set by  $R_3$ , and the output is available at a low impedance,  $V_{OUT}$ . The gain of this stage at 1kHz is defined by the RIAA curve and resistors  $R_1$  and  $R_3$  (where  $R_1$  is part of network N1), and is:

$$G_{(1\text{kHz})} = 0.101 \left( 1 + \frac{R_1}{R_3} \right) \quad \text{Eq. 8.7}$$

where 0.101 is the RIAA constant,  $K_{\text{RIAA}}$ .

An ideal RIAA response falls with increasing frequency, and will be less than unity at some high frequency. The basic topology of Figure 8.15 cannot achieve this, as the minimum gain approaches unity at some (high) parasitic zero frequency, where the network equivalent series capacitive impedance becomes equal to  $R_3$ .

However, the practical consequence of this may or may not be of significance, depending upon where the zero frequency falls. If this is well above audibility ( $\geq 100\text{kHz}$ ), it will introduce some equalization error at the upper end of the audio range, but this may be small. If this frequency is as low as 100kHz, the (uncorrected) error at 20kHz is about 0.3dB.

Fortunately, this error can be exactly compensated by a passive low-pass filter after the amplifier,  $R_5$ - $C_3$ . The time constant of this filter is set to match the time constant of the zero,  $T_4$ , which is:

$$T_4 = R_3 \times C_{\text{EQUIV}} \quad \text{Eq. 8.8}$$

where  $R_3$  is a value required for gain in the specific design, and  $C_{\text{EQUIV}}$  is the series equivalent capacitance of network capacitors  $C_1/C_2$ , or:

$$C_{\text{EQUIV}} = \frac{C_1 C_2}{C_1 + C_2} \quad \text{Eq. 8.9}$$

For example, if  $C_{\text{EQUIV}}$  of network N1 is 7.6nF and  $R_3 = 200\Omega$ , the required  $R_5$ - $C_3$  time constant is  $T = 1.5\mu\text{s}$ , which can be compensated with  $R_5 = 499\Omega$  and  $C_3 = 3\text{nF}$ . Note that this design step increases the output impedance of the circuit, making it more susceptible to load variations. Therefore this measure should be weighed against the added parts complexity and the loading tradeoffs.

In some designs, a resistor  $R_4$  (dotted) may be used in series with N (for example, for purposes of amplifier stability at a gain higher than unity). With  $R_4$  present, time constant  $T_4$  is calculated as:

$$T_4 = (R_3 + R_4) \times C_{\text{EQUIV}} \quad \text{Eq. 8.10}$$

and the  $R_5$ - $C_3$  product is then chosen to be equal to this  $T_4$ .

## Passively Equalized RIAA Preamp Topology

Another design approach is a so-called passively equalized preamp.<sup>[10]</sup> A basic circuit which can be used for such RIAA phono applications is shown in

Figure 8.16. This consists of two high quality wideband gain blocks, U1 and U2, separated by a three terminal network, "N" (either network N1 or N2).

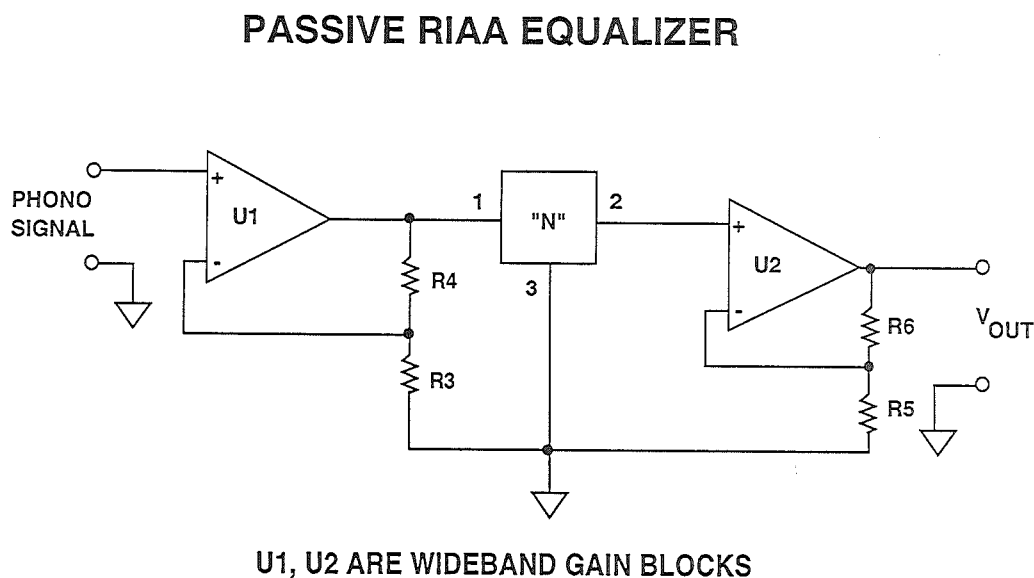


Figure 8.16

The gain stages are set up for the required total gain, with  $R_4$ - $R_3$  and  $R_6$ -

$R_5$ . In general, the 1kHz gain of this circuit is:

$$G_{(1\text{kHz})} = 0.101 \left( 1 + \frac{R_4}{R_3} \right) \left( 1 + \frac{R_6}{R_5} \right) \quad \text{Eq. 8.11}$$

The op-amp gain blocks could be made identical for purposes of simplicity but are not necessarily. A preamplifier topology such as this must be optimized for signal-handling capability, both from an overload standpoint and for low noise. Stage U1 is chosen for a gain sufficiently high that the input-referred

noise will mostly be due to this stage and the cartridge, but yet not so high that it will clip at high-level high-frequency inputs. Amplifiers with a 10V rms output capability ( $\pm 18\text{V}$  supplies) allow U1 to accept  $\approx 400 \text{ mV}_{\text{rms}}$  with a gain of 25 at high frequencies.

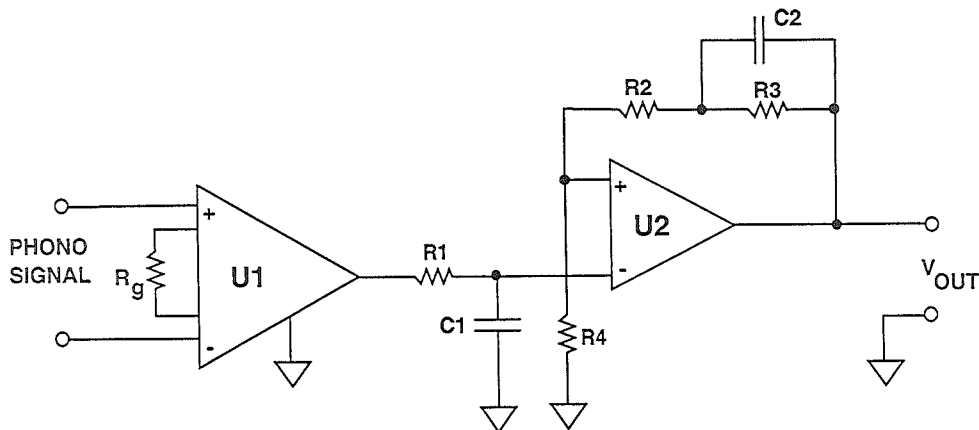


### Hybrid Equalized RIAA Preamp Topology

By using a combination of passive/active or “hybrid” equalization, the noise/overload constraints of the totally passive equalization is lessened.<sup>[15]</sup> In

addition, “hybrid” equalization can use either an instrumentation or an op amp input stage for best noise performance (Figure 8.17).

## HYBRID (PASSIVE AND ACTIVE FEEDBACK) RIAA EQUALIZER



■ U1, U2 ARE WIDEBAND GAIN BLOCKS

■ U1 CAN BE AN INSTRUMENTATION AMP OR AN OP AMP

$$T_1 = R_3 \cdot C_2 = 3180\mu s$$

$$T_2 = \frac{R_3 \cdot C_2 (R_2 + R_4)}{R_2 + R_3 + R_4} = 318\mu s$$

$$T_3 = R_1 \cdot C_1 = 75\mu s$$

Figure 8.17

Here U1 is shown as a differential input amplifier, which accepts a balanced signal from the phono cartridge, and amplifies it by a wideband gain of  $G_{(U1)}$  (which is the gain of the device

used for U1). Overall, the gain of this entire circuit is the product of the U1-U2 stage gains, as modified by the RIAA frequency response. At 1kHz, the gain is:

$$G_{(1kHz)} = 0.101 [G_{(U1)}] \left( 1 + \frac{R_2 + R_3 + R_4}{R_4} \right) \quad \text{Eq. 8.12}$$

Unlike the previous equalizers, the three time constants in this circuit are not set by a single network, but by the relationships shown in the Figure 8.17. This has the advantage of less interaction, and noise performance can be

optimized by using less gain in stage U2. The gain of stage U1 in this circuit ( $G_{(U1)}$ ) is used to adjust overall gain, whether U1 is an in-amp, or a conventional op amp stage.

## Active Feedback RIAA Phono Preamp

Figures 8.18 and 8.20 illustrate two variants of the most popular approach to achieving a simple RIAA phono preamp using active feedback. Figure 8.18 is a high-performance DC coupled version using the recommended precision components. Amplifier U1 provides

the gain, and equalization components  $R_1$ - $R_2$ - $C_1$ - $C_2$  form the RIAA network, providing a very accurate realization with standard component values. (The network used here is N1 of Figure 8.14a, with terminals 1 and 3 common and values scaled 10x).

## ACTIVE FEEDBACK RIAA PREAMP (DC COUPLED)

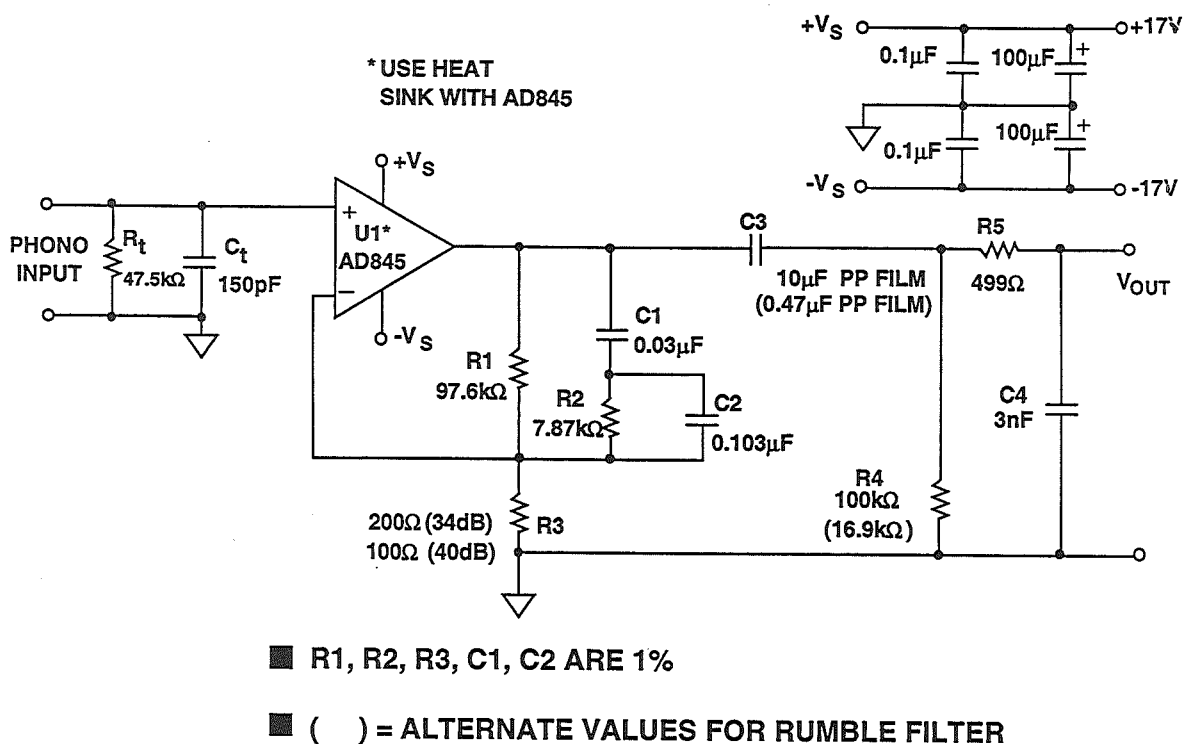


Figure 8.18

The actual network components should be 1% precision high-quality types, both for initial equalization accuracy and also for minimal errors from parasitic properties. High-quality metal-film resistors and film capacitors of polystyrene or polypropylene are recommended.

The input RC components,  $R_t$ - $C_t$ , terminate the moving magnet cartridge with values recommended by the manufacturer. The values shown are typical, with  $C_t$  variable for flattest response. Note that these comments apply generally to all the RIAA circuits that follow.

The amplifier parameters required for optimum performance of this circuit are demanding. For lowest noise from the cartridge's inductive source, the amplifier should have a voltage noise density of 5 nV/ $\sqrt{\text{Hz}}$  or less, and a current noise density of 1 pA/ $\sqrt{\text{Hz}}$  or less. The former requirement is best met by using low-noise bipolar-input amplifiers, such as the OP-27, OP-270, OP-275, and SSM-2134 or 5532/5534 types. The latter need is best met by the use of FET-input amplifiers in general.

For bipolar-input amplifiers, DC input-bias current can be a potential problem when direct coupling to the cartridge, so in this directly coupled circuit an op amp with a low input bias current amplifier is suggested. If a bipolar input amplifier is used for U1, it should have an input current of  $\leq 100\text{nA}$  for minimum problems with DC offset (assuming a typical phono cartridge of about 1k $\Omega$  resistance). Examples here are the OP-27, OP-270 and related devices.

FET-input amplifiers generally have negligible bias currents but they also tend to have a higher voltage noise. FET-input types useful for U1 are the AD845 and SSM-2131, even though their voltage noise is not as low as the best of the bipolar devices mentioned. On the positive side, they both have a high output current and slew rate for low distortion when driving the load of the feedback network (which approaches  $R_3$  at high frequencies). Of the two, the SSM-2131 has the lower voltage noise, while the AD845 has higher output current and slew rate.

For high-gain accuracy, particularly at high stage gains, the amplifier should have a high gain-bandwidth product; preferably 5 MHz or more. Because of the 100% feedback through the network at high frequencies, the amplifier used for U1 must be a unity-gain-stable type. To minimize noise from sources other than the amplifier, gain resistor  $R_3$  is set to a relatively low value, and generates a voltage noise that is low in relation to that of the amplifier used.

The 1kHz gain of this circuit can be calculated from Eq. 8.7 above. For the values shown, the gain is just under 50 times ( $\approx 34\text{dB}$ ). Higher gains are easily accommodated by decreasing  $R_3$ , but gains higher than 40dB may show increasing equalization errors, depending upon the gain bandwidth of the amplifier used. For example,  $R_3$  can be 100 $\Omega$  for a gain of about 100 times ( $\approx 40\text{dB}$ ) (note that if  $R_3$  is changed for a higher gain,  $C_4$  should also be changed to satisfy Eq. 8.8).

With a suitable amplifier, this circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms (assuming  $\pm 15\text{V}$  supplies) and higher with the  $\pm 17\text{V}$  supplies suggested. RIAA accuracy is quite good using the stock equalization values, and a simulation run is shown in Figure 8.19 for the suggested gain of 34dB. In this expanded scale plot over the 20-20kHz range, the error relative to the 1kHz gain is less than  $\pm 0.1\text{dB}$ .

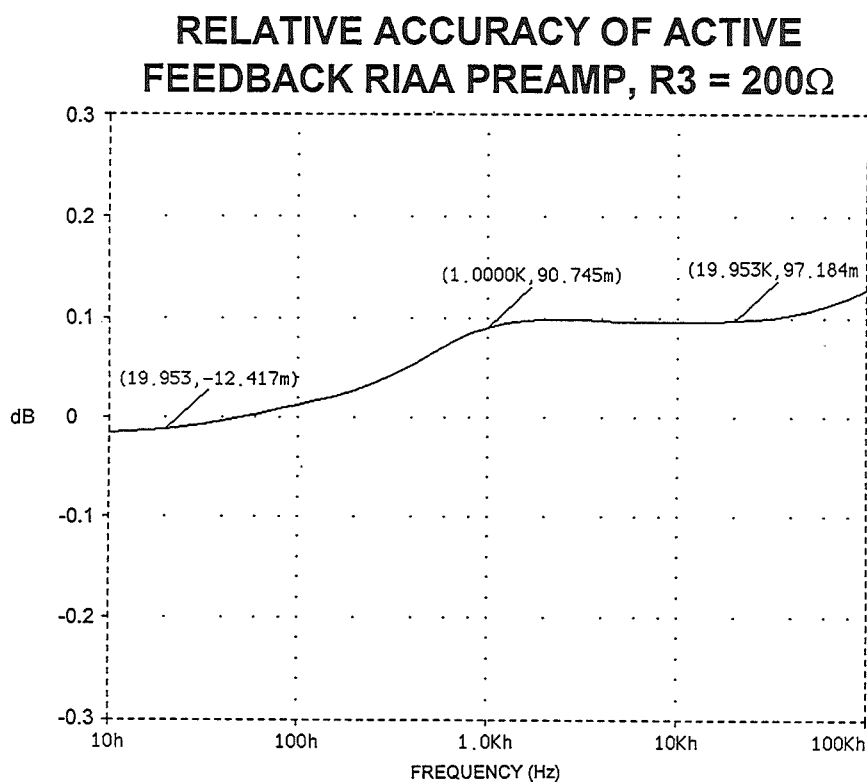


Figure 8.19

For extended low-frequency response,  $C_3$  and  $R_4$  are the larger values shown, with  $C_3$  preferably a polypropylene film type. Alternately, the smaller values for  $C_3$  and  $R_4$  (when applied) form a simple 6dB per octave rumble filter, with a corner at 20Hz. Placing a rumble filter's high-pass action after the preamp stage has the desirable property of discriminating against the RIAA amplified  $1/f$  noise components, in addition to the pickup produced disturbances.  $C_3$  is the only DC blocking capacitor in the circuit. Because the DC gain of the circuit is on the order of 54dB, the amplifier used must be a low offset-voltage device, with an offset voltage that is insensitive to the source. This

implies an offset voltage on the order of a few mV, and a low bias current.

Since this is a high-gain low-input-level circuit, the supply voltages should be well regulated and free of noise, and reasonable care should be taken with the shielding and conductor routing.

An alternative AC coupled form of this circuit can be built with higher bias current, low-noise bipolar devices, such as the OP-275 with  $I_B = 350\text{nA}(\text{max})$ , which would otherwise make direct coupling to a cartridge difficult. This form of the circuit is shown in Figure 8.20, and can be used with any unity gain stable bipolar op amp.

## ACTIVE FEEDBACK RIAA PREAMP (AC COUPLED)

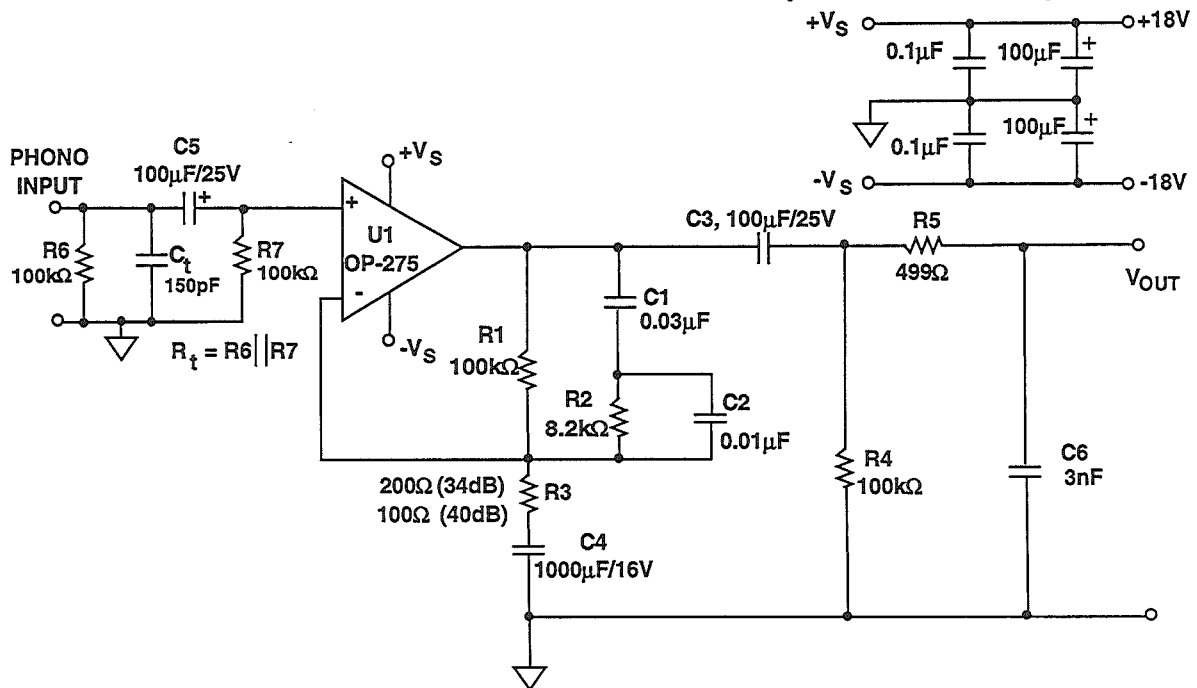


Figure 8.20

Here input AC coupling to U1 is added with C<sub>5</sub>, and the cartridge termination resistance R<sub>t</sub> is therefore made up of the parallel equivalent of R<sub>6</sub>-R<sub>7</sub>. R<sub>3</sub> of the feedback network is AC-grounded via C<sub>4</sub>, a large value electrolytic. These measures reduce the DC offset at the output of U1 to a few mV. Nearest 5% value units are also used for the network components, making the design both easily reproducible and inexpensive. The output coupling network C<sub>3</sub>-R<sub>4</sub> is shown with values suitable for wideband response, but if desired, can

be altered to a 7950μs time constant for use as a 20Hz rumble filter. The R<sub>3</sub>-C<sub>4</sub> time constant shown provides a corner frequency of ≤1Hz.

The frequency response of this version is not quite as good as that of the circuit in Figure 8.18, but is still within ±0.2dB over 20Hz-20kHz (neglecting the effects of the low frequency rolloff). If tighter response is desired, the N1 values can be used. For the OP-275, supplies can be increased to ±21V if desired, for outputs up to 10Vrms.

### Passively Equalized RIAA Phono Preamp

Another area of interest is passively equalized preamplifier circuits used with phono signal sources. A circuit useful for such RIAA phono applications is shown in Figure 8.21. This circuit

consists of two high-quality wide bandwidth gain blocks, U1 and U2, as discussed in basic form in Figure 8.16.

### PASSIVELY EQUALIZED RIAA PREAMP

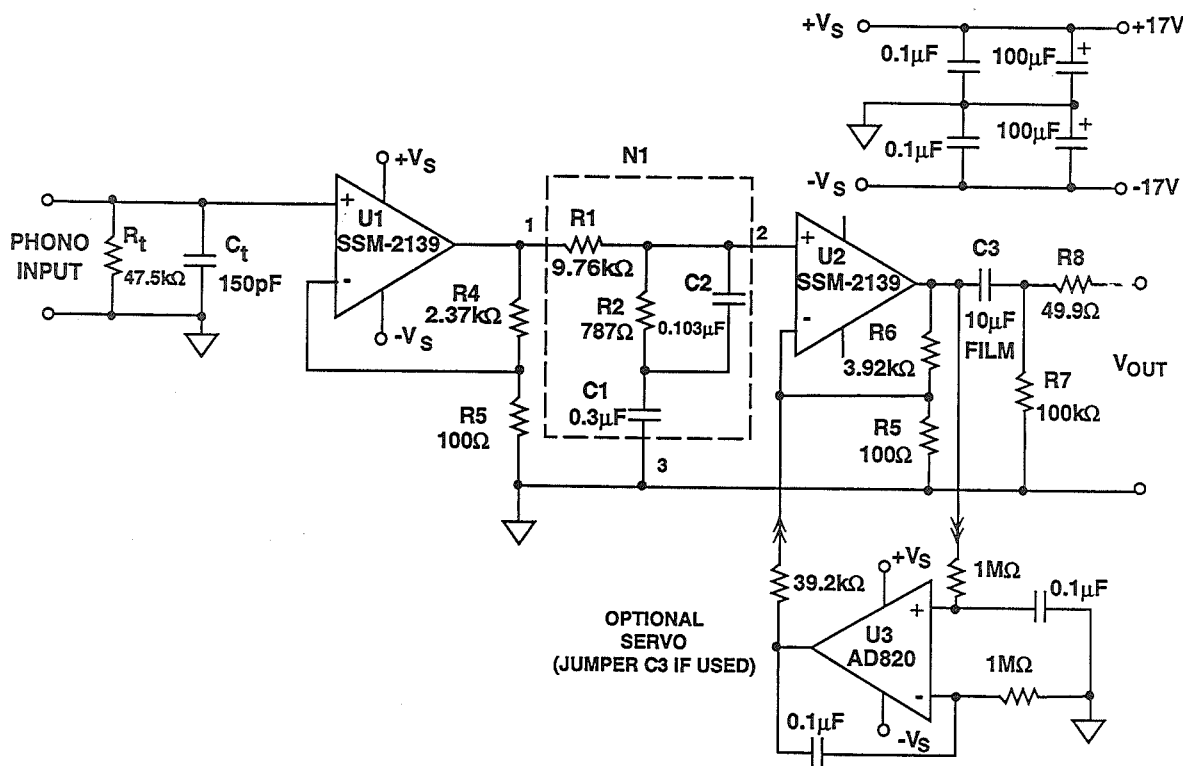


Figure 8.21

The gain of the two blocks are set up by  $R_4$ - $R_3$  and  $R_6$ - $R_5$ , as defined in Eq. 8.11. The values shown yield a 1kHz gain that is the product of the U1-U2 stage gains (24.7 times 40.2), times that of the interstage network N. With the 1kHz RIAA gain factor of 0.101, this yields an overall 1kHz gain of 40dB. Other gains can be realized by changes to  $R_4$ .

A passively equalized preamplifier such as this one must be carefully optimized

for signal handling, both from an overload standpoint and for low noise. Stage U1 is chosen for a gain sufficiently high that the input-referred noise will mostly be due to this stage (and the cartridge, when connected), but yet not so high that it will clip high-level high-frequency inputs. To aid this objective, maximum supply voltage and a high output capability amplifier should be used.

Since U1 operates at a relatively high gain, it need not necessarily be unity gain stable. Decompensated low noise op amps such as the OP-37, SSM-2139, and the FET input AD745 may provide better signal/noise ratio in this application. Other FET-input types, the AD845, the SSM-2131, and OP17 or PM357 types will yield good performance, but with higher noise levels. However, perhaps the best choice is the SSM-2139 dual, which performs both U1 & U2 functions, and has excellent DC specifications.

Gain distribution between U1 and U2 should be LOW/HIGH from an overload standpoint, but HIGH/LOW from a noise standpoint. Practically, these conflicting requirements can be eased by choosing a low noise device for U1, and using the highest possible power supply voltages. There is nearly 40dB loss in the network N at 20 kHz, so output overload of the circuit will be noticed at high frequencies first. With the gain distribution chosen, the circuit allows a 3V rms undistorted output to 20kHz with  $\pm 15V$  supplies, and more with higher supply voltages.

The equalization network N following U1 should use the lowest impedance values practical from the standpoint of low noise, as the noise output at pin 2 of the network is equivalent to the input referred noise of A2. A practical example for this network are the "N1" RC values of  $R_1$ - $R_2$ - $C_1$ - $C_2$  in Figure 8.14a. As noted, scaling can be applied to either network of Figure 8.14 for component selection, as long as the same ratios are maintained. If extremely low

noise performance is sought, such as is required for a moving coil preamp, then the N1 values can be reduced further.

Noise in amplifier U2 is less critical than in U1 at low frequencies, but is still not negligible. A low voltage noise device is very valuable for U1 and U2, as is a relatively low input current noise.

U1 should have a low bias current. With 100nA or less bias current, direct coupling to a moving magnet phono cartridge is practical. For example, the maximum 80nA bias current of the SSM-2139 will induce only an 80-160 $\mu$ V input voltage offset at U1 for a typical 1-2k $\Omega$  cartridge resistance. Similarly, the bias current induced offset voltage of U2, from the 10k $\Omega$  DC resistance of  $R_1$  will be low relative to the amplified offset of U1. As a result, the worst-case overall output DC offset using the SSM-2139 can be held to under 1V for a 40dB gain, allowing the use of a single coupling capacitor,  $C_3$ , for DC blocking purposes.

Frequency response of this passively equalized preamp is better than the active version, because there is less interaction with the amplifier(s) compared to the active topology. The frequency response can approach the inherent accuracy of the network components in the audio range, with greater errors at higher frequencies. Figure 8.22 illustrates this point in a simulation of the Figure 8.21 circuit using OP-37 models. Midband error is on the order of  $\pm 0.02$ dB with the N1 network composite values.

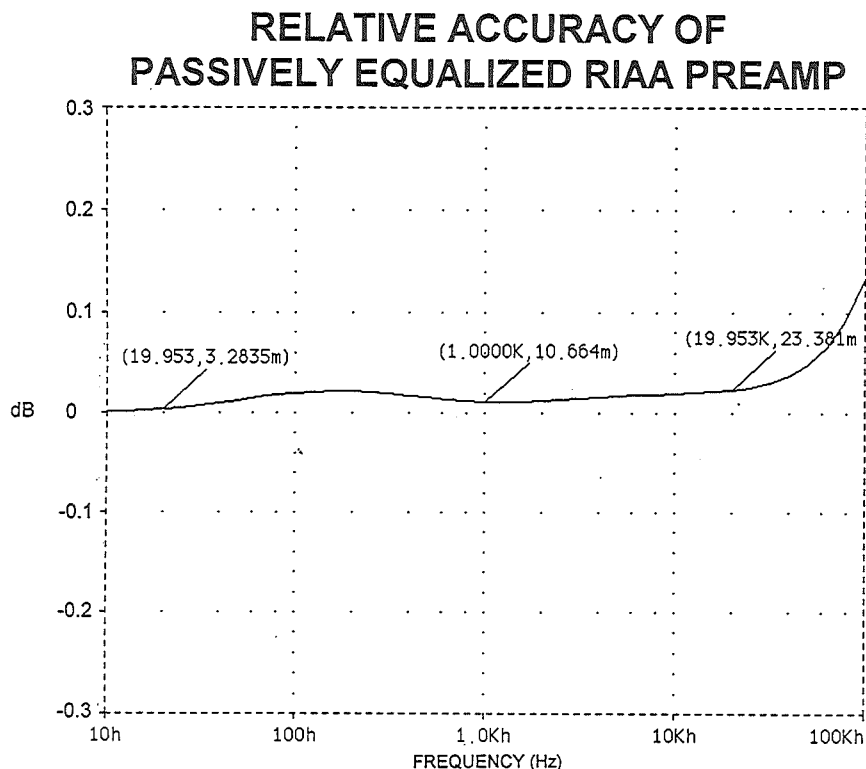


Figure 8.22

This circuit also can be adapted to servo control of the output offset, by replacing  $C_3$  with the optional noninverting servo integrator around stage U2, shown as an option in Figure 8.21.

A general-purpose noninverting servo described in the appendix can be used, along with a low-offset op amp such as the AD820, AD711, OP-97 or AD705.

### Hybrid-Equalized Differential-Input, Servo-Controlled, RIAA Phono Preamp

By using a combination of passive and active equalization, some of the noise/overload constraints of totally passive equalization are reduced. In addition, this “hybrid” equalization can be combined with a low-noise differential-input instrumentation amplifier, the AD625, for excellent noise performance and flexibility.

Figure 8.23 shows a hybrid-equalized phono preamp circuit, which has servo

control for precise offset and the elimination of coupling capacitors. U1 is the AD625, an in-amp with low voltage noise ( $4\text{nV}/\sqrt{\text{Hz}}$ ). It is used as an adjustable differential input amplifier, which accepts a balanced signal from a moving magnet cartridge. Both the DC and AC terminations of the cartridge are split and balanced, with an optional AC trim for best HF CM rejection ( $C_{tb2}$ ).



## HYBRID EQUALIZED RIAA PREAMP

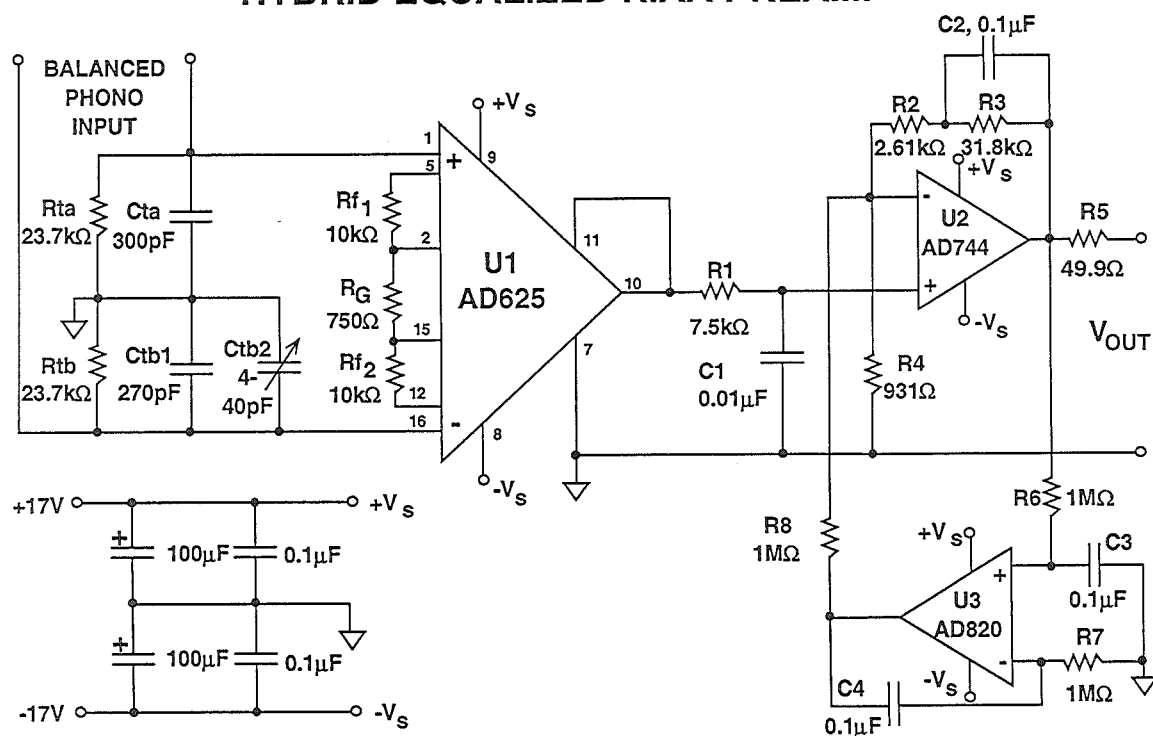


Figure 8.23

The common-mode rejection of U1 below 100 Hz is on the order of 100 dB, a great aid to noise rejection. To minimize noise pickup, a shielded twisted-pair signal cable should be used from the cartridge, with the shield grounded to the common point of  $R_{ta}$ - $R_{tb}$  as shown.

The gain of stage U1 in this circuit is:

$$G(U1) = 1 + \frac{2R_F}{R_G} \quad \text{Eq. 8.13}$$

where  $R_{F1} = R_{F2}$ , and these resistors and  $R_G$  are located at pins 5-2, 2-15, and 15-12 of the AD625.  $R_{F1}$  and  $R_{F2}$  are matched 10kΩ 1% metal film types.  $R_G$  is also a 1% metal-film resistor that is used to adjust overall gain as necessary.

The gain of this entire circuit is the product of the U1 and U2 stage gains, as modified by the RIAA frequency response. At 1kHz, the gain is:

$$G_{(1\text{kHz})} = 0.101 \left( 1 + \frac{2R_F}{R_G} \right) \left( 1 + \frac{R_2 + R_3 + R_4}{R_4} \right) \quad \text{Eq. 8.14}$$

With the values shown, the gain is about 40 dB, but it can be adjusted by  $R_G$ . The  $R_2$ - $R_4$  values should not be altered, since they set the two lower frequency RIAA time constants (3180  $\mu\text{s}$  and 318  $\mu\text{s}$ ). The 75  $\mu\text{s}$  time constant is set by  $R_1$ - $C_1$ .

Because this topology separates the definition of time constants T1-T2 and

T3 into different networks and the interaction of T1-T2 with op amp U2 is low, this preamp is capable of excellent frequency response. By using standard values for  $C_1$ - $C_2$ , time constants T1-T3 are set easily with resistors; then T2 is set with only slightly more complexity. The end results are excellent, as the simulation of Figure 8.24 indicates.

## RELATIVE ACCURACY OF HYBRID EQUALIZED RIAA PREAMP

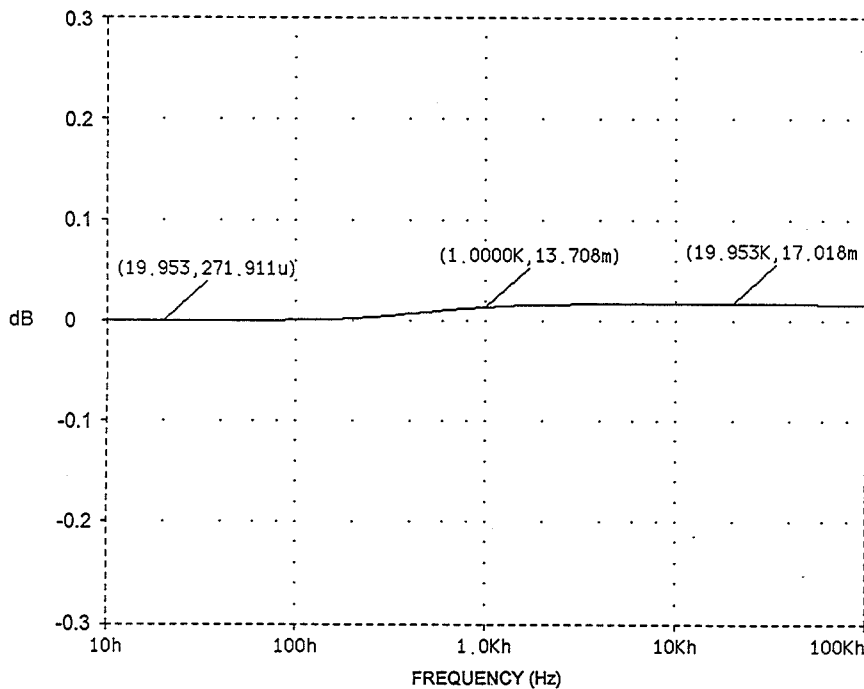


Figure 8.24

Amplifier U3 is a DC servo stage, using an AD820 in a noninverting configuration with an effective 0.3 second time constant. DC feedback for the servo is through the feedback input of stage A2. Note that if any op amp other than the AD820 is used for U3, it is prudent to check if low leakage diodes will be needed as servo anti-latchup clamps across  $C_3$  (discussed in the appendix). The output offset of the circuit will be essentially that of U3, typically less than 1 mV.

Single devices are shown for U2-U3, each optimized for the function. Use of the AD744 for U2 allows very low

distortion from this stage, and the AD820 is an effective servo amplifier. Duals will be more cost effective in some applications, however, and an AD712 or OP-249 can be used for U2-U3 (clamping diodes may be necessary at U3).

This circuit is capable of very high performance with excellent SNR. Very careful circuit layout is necessary around the input of stage U1, the feedback components at U2, the high-impedance inputs of U3, and components  $R_6$ - $R_7$  and  $C_3$ - $C_4$  should be close to U3.

### Moving Coil RIAA Preamplifiers

There are two general approaches which may be taken to satisfy the amplification requirement of a moving coil cartridge. These consist of two different methods by which the additional voltage gain required by the moving coil pickup may be achieved.

One technique is to use another low noise, flat, wideband preamp, ahead of an existing RIAA-equalized preamp. Such an amplifier stage is called a "pre-preamp" (also sometimes called a "head amp," for its place at the head of the signal path). A second technique is to

incorporate the very high gain required directly into an RIAA equalized stage.

A pre-preamp circuit useful with any standard RIAA preamp is shown in Figure 8.25. Because of the extremely low source resistance from which this type of circuit must operate ( $\approx 10$ - $100\Omega$ ), amplifier feedback resistances must be kept very low. Obviously, the input voltage noise of the amplifier used must also be low, in general  $\leq 1\text{nV}/\sqrt{\text{Hz}}$ . Two devices which have noise voltages this low are the AD797 op amp, and the SSM-2017 in-amp.

## SINGLE-ENDED RIAA "PRE-PREAMP" WITH 30/40dB GAIN

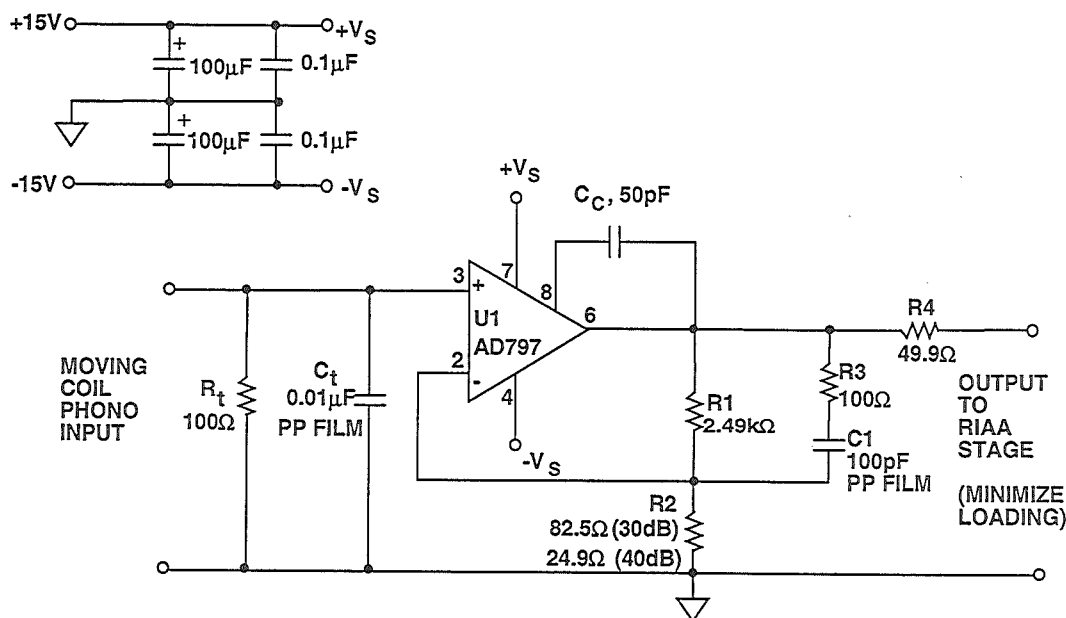


Figure 8.25

The circuit of Figure 8.25 is a pre-preamp suitable for low level input single ended applications. It uses an AD797 op amp in a low noise configuration, with either 30 or 40dB gain, adjustable by  $R_2$ . At the higher (40dB) gain the output noise of this circuit will be dominated by the source or the op amp, dependent upon the actual DC resistance of the cartridge in use. With a low resistance cartridge, it will be on the order of  $2\text{nV}/\sqrt{\text{Hz}}$ .

Input terminating resistor  $R_t$  should be adjusted to suit the cartridge.  $C_t$  is relatively non-critical, but should be a low inductance film type to minimize RFI effects. Capacitor  $C_c$  acts as part of a distortion cancellation loop, in conjunction with the AD797's internal stages.

In a system, this circuit can be used two ways. One is as a stand-alone pre-preamp, used with another RIAA preamp, in which case a short low capacitance cable connects the output to that stage, and  $R_2$  is set for the desired overall gain. Another way to use this circuit is as the first stage in either a passive or hybrid RIAA equalizer circuit, for example as a U1 stage replacement in either Figure 8.21 or Figure 8.23.

This entire stage replaces the entire U1 stage in one of those circuits, and  $R_1$ - $R_2$  are adjusted for the desired 1kHz gain. Typically this will be of the order of 50-60 dB, or about 20 dB higher than with the moving magnet transducer.

Taking the passive equalizer of Figure 8.21 as an example: the gain of stage U1 becomes 5-20 times higher, making it in the range of 100-400 times. For an overall gain of 54dB,  $R_2$  of Figure 8.25 should be  $20\Omega$  for a U1 stage gain of about 125 times, or 42dB. Combined with the N1 network and stage U2 of Figure 8.21, the overall gain is then  $\approx 510$  times, or close to 54dB. The gain expression generally follows Eq. 8.11, but with the values of  $R_1$  and  $R_2$  from Figure 8.25 used in place of  $R_4$  and  $R_3$ . The resistor shown in Figure 8.25 as  $R_4$  then becomes the input resistance of the network N1, with the remainder of the circuit similar to Figure 8.21.

The AD797 is a stable DC amplifier, but with an input offset of  $\pm 80\mu\text{V}$  and cascaded DC gains above 1000, some form of overall DC stabilization will be needed. If it is used in the circuit of Figure 8.21, a DC servo should be used with the loop adjusted to null out the input referred offset which is  $\pm 150\mu\text{V}$ . The output amplifier can be a buffered composite amp using the AD744 and the AD811, as described in the "Line Drivers" discussion. Details of this configuration are left as an "exercise for the reader".

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## TAPE PREAMPLIFIERS

A third audio preamplifier application is a magnetic tape or film playback system. These preamp circuits often operate at signal levels of 1 mV or less, placing stringent SNR requirements on the amplifier. In addition to high 1kHz

gain, equalized frequency response is also necessary, which can raise the low-frequency gain as high as 80 dB. Few op amps can provide adequate loop gain with low input noise and high linearity under these conditions.

### Tape Playback Basics

A generalized post-emphasis response curve required for tape playback is shown in Figure 8.26, similar in some senses to the generalized RIAA response of the previous section. These curves correspond to a subset of various

tape playback response characteristics which meet the requirements of the IEC standard.<sup>[1]</sup> They are expressed here in dB relative to response at DC, over a range of 10Hz-100kHz.

8

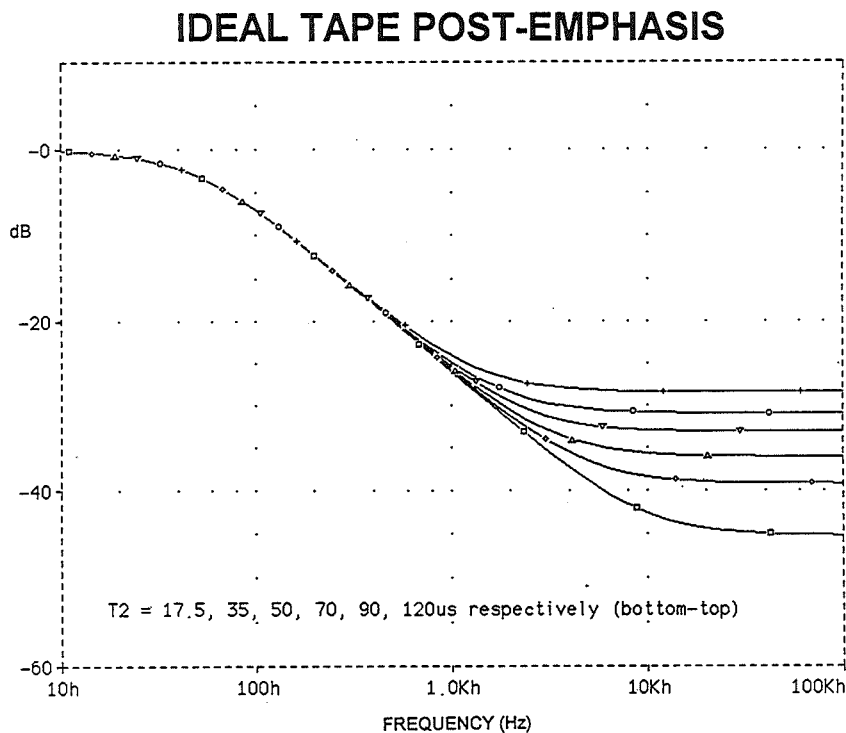


Figure 8.26

From Figure 8.26 gain is maximum below 50 Hz ( $f_1$ ), which is the lower corner frequency beginning the equalized portion of this curve, corresponding in this case to a 3180 $\mu$ s time constant, T1. (Note: as was true for the RIAA time constants of T1-T3, tape time constants T1-T2 are described here as they correspond to ascending frequency, the reverse of the terminology in [1]. The time constants themselves are identical). One major difference between RIAA and tape playback equalization is that there are many standard tape time constants, two for low frequencies and 5 for high frequencies, which can be combined differently. The discussions which follow place the similarities between RIAA and tape in context, then address the many differences necessary for tape equalization.

Above 50Hz, the response rolls off at 6 dB/octave until it reaches a corner frequency  $f_2$ , determined by time constant T2. This time constant will vary according to tape speed, but will generally be in a range of 17.5-120 $\mu$ s (Figure 8.26).

At the reference frequency of 1 kHz, preamp gain can be in the range of 40 to 50 dB. Another frequency of interest is  $f_0$ , the low-end rolloff frequency, somewhere below 50 Hz and not shown explicitly by Figure 8.26. An exact choice for this frequency is left to the designer, in light of specific requirements and the applicable standards. What has been described thus far is what could be termed a "two time constant" tape equalizer, where T1 is 3180 $\mu$ s, and T2 is one of the time constants noted. The specific case of 3180 $\mu$ s/50 $\mu$ s is known as NAB equalization, and used in a design example.

While the tape playback EQ curves of Figure 8.26 may appear similar to the analogous RIAA curves, this similarity is more superficial than fundamental. For the cases so far described, it is true that a tape playback amplifier can be modeled as a low pass amplifier (like the RIAA case, but with a single pole and zero). The design process to follow shows how to use these factors to advantage for a specific pair of time constants and gain.

However, the two time constant case is not the entire picture for tape EQ, as the low frequency time constant T1 can actually be extended towards DC. This makes the present design process less predictable. There are also other potential parasitic effects on the system, including the loading of the tape head, which should be addressed at some point during the design.

A greater appreciation for how the tape playback EQ operates is gained if it is broken down into its basic factors. Assuming an ideal head, the playback signal for a constant tape flux is the derivative of the flux. It follows that the tape playback amplifier should have an integrating response. The tape standards call for a flux falling with increasing frequency above 1325 to 9000Hz, depending upon speed. Playback integration is always modified to boost gain at high frequencies. T2 is always present in some form, which implies that the integration is stopped at some high frequency, corresponding to  $1/2\pi T_2$ .

Some standard equalizations call for boosting low frequency response in recording. In this case T1 is present, and integration is stopped at a low



frequency,  $1/2\pi T_1$ . For cases without low frequency boost,  $T_1 \Rightarrow \infty$ , and the integration continues down until limited by circuit practicalities.

Many non-ideal factors related to the tape pickup head may also require correction. These include non-uniformity of frequency response (eddy-current losses, RC head loading), wavelength response (gap-length loss, head bumps), lot-lot variability, etc. Most

tape playback EQ circuits therefore provide trims for one or more head design parameters, to accommodate these limitations and to allow best overall calibration. This process involves playback of a standard test tape through the system, chosen for the standard involved.<sup>[1,2]</sup> In view of the above factors, a "universal" tape playback EQ circuit is impossible, and a well designed practical circuit should make allowances for external factors.

### A "Two Time Constant" Design Example

A flexible tape preamp with a range of possible uses is shown in Figure 8.27. This circuit is most effective with only a few selected op amps, preferably a low

noise, decompensated FET input type such as the AD745, or possibly either of the low noise bipolar input OP-37 or SSM-2139.

8

### TAPE PREAMPLIFIER

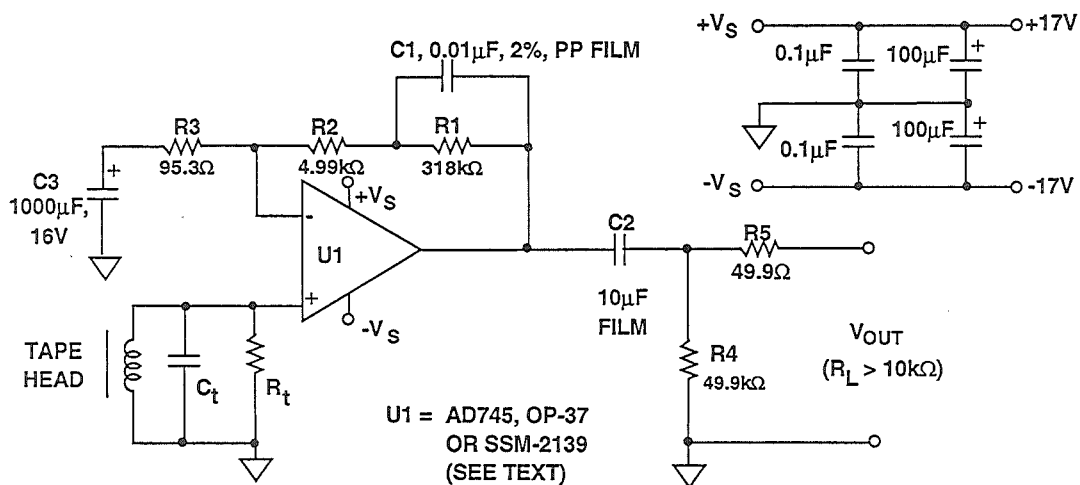


Figure 8.27

This preamp design has a high frequency gain greater than unity, due to the presence of T2 and can therefore take advantage in the extended bandwidth and low SNR in a decompensated amplifier. Possible alternates and further selection criteria are discussed below. This circuit may be used as it stands, or with other component values for specific time constants and/or gains.

The gain and equalization characteristics of this circuit are set by the feedback network, which consists of  $R_1$ - $R_3$  and  $C_1$ . The interactions of these components are best appreciated when analyzed as a network, as was done for RIAA preamps. In this case, two time constants are involved, T1 and T2, but the general design approach is similar to that for an RIAA active feedback preamp.

In the circuit of Figure 8.27, time constants T1 and T2 are set as:

$$T1 = R_1 C_1 \quad \text{Eq. 8.15}$$

and,

$$T2 = \frac{R_1 C_1 (R_2 + R_3)}{R_1 + R_2 + R_3} \quad \text{Eq. 8.16}$$

For many tape playback circuits, T1 is fixed at 3180 $\mu$ s, so  $R_1$ - $C_1$  can be set to convenient values, here 0.01 $\mu$ F and

318k $\Omega$ . Time constant T2 will be unique to a given playback speed, so Eq. 8.16 above is solved for this case. The T2 of 50 $\mu$ s used yields  $R_2 = 4.99$ k $\Omega$ .

The ratio of  $(R_1 + R_2 + R_3)$  to  $R_3$  determines the gain at DC (similar to the RIAA case), so the nominal 1kHz gain and T2 are somewhat interactive. In practice however, small variations in  $R_3$  have minimal effect on the frequency response.

For equalization using the 3180 $\mu$ s time constant, the 1kHz gain can be related to an (ideal) DC gain, since the stage is a low pass amplifier with a pre-defined response. For a T2 of 50 $\mu$ s the DC/1kHz difference is 25.61 dB. For other T2 and a given 1kHz gain, the DC gain can be calculated, so that given the desired gain at 1kHz, it is then possible to select the  $R_1$ - $R_3$  ratios.

It is generally convenient in this design process to relate the DC/1kHz relative gains in terms of the equivalent 1kHz scaling coefficient, "K", where K is unique to a given T2, or " $K_{(T2)}$ ". In the 3180 $\mu$ s/50 $\mu$ s case, the 1kHz 25.61 dB loss relative to DC corresponds to a  $K_{(T2)}$  of 0.0524. When this coefficient is multiplied by the DC gain, it gives the 1kHz numeric gain for the value of T2 in use, which is:

$$G_{(1\text{kHz})} = K_{(T2)} \left( 1 + \frac{R_1 + R_2}{R_3} \right) \quad \text{Eq. 8.17}$$

Or for the example of  $T_1/T_2 = 3180\mu\text{s}/50\mu\text{s}$ , the 1kHz gain is:

$$G_{(1\text{kHz})} = 0.0524 \left( 1 + \frac{R_1 + R_2}{R_3} \right) \quad \text{Eq. 8.18}$$

Since the time constants should be the first variables to be resolved in the design process,  $R_3$  remains for the overall network gain adjustment, after  $R_1$ - $R_2$  are selected. Given a gain at 1kHz of  $G_{(1\text{kHz})}$  and the scaling coefficient  $K_{(T_2)}$  for the  $T_2$  in use,  $R_3$  can be calculated from:

$$R_3 = \frac{R_1 + R_2}{\frac{G_{(1\text{kHz})}}{K_{(T_2)}} - 1} \quad \text{Eq. 8.19}$$

In this  $3180\mu\text{s}/50\mu\text{s}$  example the 1kHz gain is 45dB, so  $G_{(1\text{kHz})}$  is 177.83, and  $K_{(50)}$  is 0.0524, thus  $R_3$  works out as  $95.3\Omega$  (nearest standard value).

Figure 8.28 illustrates the relative accuracy of this NAB tape equalizer using the chosen component values and an AD745 op amp model in a SPICE simulation. The 45 dB gain is accurate

within 0.1dB at 1kHz, and the frequency response errors of the circuit relative to the ideal  $3180\mu\text{s}/50\mu\text{s}$  time constants are within  $\pm 0.1\text{dB}$  over 20Hz-20kHz (not shown). Similar results should be expected using other  $T_2$  options. Figure 8.29 lists time constants from 30-120 $\mu\text{s}$ , and their corresponding scaling coefficients.

8

### NAB 50 $\mu\text{s}$ POST-EMPHASIS CIRCUIT, $R_1$ = VARIOUS VALUES

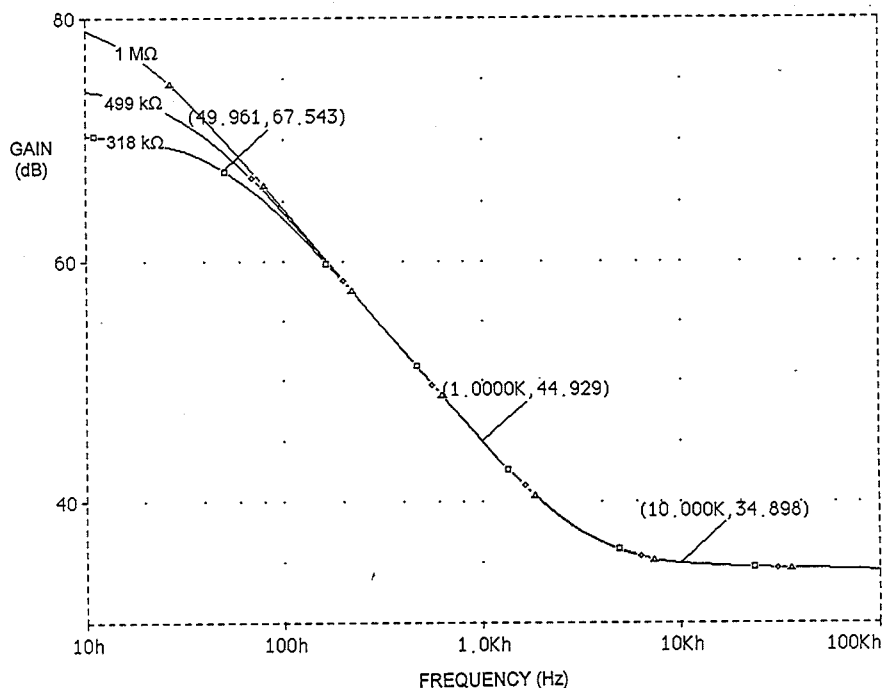


Figure 8.28

### 1KHZ SCALING COEFFICIENTS FOR TAPE EQUALIZERS FOR T2 = 17.5, 35, 50, 70, 90, AND 120 $\mu$ s

T2, $\mu$ s	K (T2)
17.5	0.0503
35	0.0512
50	0.0524
70	0.0546
90	0.0574
120	0.0626

Figure 8.29

#### T1 > 3180 $\mu$ s

While the situation just described covers the 3180 $\mu$ s/50 $\mu$ s and other T2 cases, some questions remain as to how to address the situation where T1 is allowed to approach  $\infty$ . This corresponds to an integrator unbounded at low frequencies, which is of course a practical impossibility. Nevertheless, this case of "T1 > 3180 $\mu$ s" EQ can also be approached in practical terms, and is also illustrated in Figure 8.28.

For the circuit of Figure 8.27 and a given gain ( $R_3$ ), the slope of integration is largely dominated by the value of capacitor  $C_1$ . As long as this capacitor is constant, the gain curve will be essentially constant above 100Hz. Therefore, raising the T1 time constant

by raising  $R_1$  has the effect of moving the low frequency pole downwards from 50Hz. In Figure 8.28, this is illustrated by the two higher gain low frequency curves, showing cases of  $R_1 = 499k\Omega$  and  $1M\Omega$ . These curves correspond to new T1's of 4990 and 10000 $\mu$ s, respectively, and for  $R_1 = 1M\Omega$ , gain is approaching 80dB at 10Hz. The corresponding turnover frequencies would be 32 and 16Hz.

While this is simple to implement conceptually, for it to be useful the op amp employed must leave adequate open loop gain. Also, other low frequency rolloffs within the circuit may possibly affect gain accuracy at the extreme low frequencies, and should be

checked. Practically speaking, when a  $T1 \rightarrow \infty$  EQ case is used, a trim for the  $R_1$  value should be provided, and the circuit time constants for  $R_3$ - $C_3$  and  $C_2$ - $R_4$  should be appreciably greater

than the effective  $T1$  value. The op amp used should have an open loop gain of one million or more, which is the case for the AD745.

### Optimizing the Remaining Circuit

Other circuit details around U1 are also important in realizing the full potential of this configuration. For lowest noise, the value of resistor  $R_3$  should be low in comparison to the source resistance. Capacitor  $C_3$  and  $R_3$  set the low frequency rolloff frequency, which is  $\leq 2\text{Hz}$  for the values shown in Figure 8.27. Output coupling capacitor  $C_2$  also sets an LF cutoff at 0.16Hz with a 10k $\Omega$  load. Note that this is the lowest recommended load for the circuit for best EQ accuracy and overall performance, unless U1 is provided with additional buffering for greater drive.

If  $R_3$  is made variable, it can provide gain trim for the circuit, varying the 1kHz gain by +5 and -4dB, about 45 dB, using a 50 $\Omega$  resistor and 100 $\Omega$  pot. *Note that wide range gain adjustment is not generally recommended, due to potential interactions with frequency response.*

For greater gain changes, a better solution is a design re-scaled around the higher (or lower) 1kHz gain, which may then be trimmed if necessary. Gain can also be trimmed in a post EQ gain stage which may also serve as a buffer amplifier.

If adjustment of  $T2$  is wanted, resistor  $R_2$  can be made variable, to accommodate the various playback curves. *However, when a decompensated amplifier is used, the minimum allowable value of  $R_2$  is  $4 \times R_3$  for stability reasons.*

Using an op amp with input offset of less than 1mV (which is the case with all those mentioned), the maximum output DC offset from U1 will be on the order of a few mV when  $C_3$  is used, since the amplifier operates with unity DC gain. This provides maximum headroom, and for  $\pm 15\text{V}$  supplies output signals of 5Vrms or more are possible, since the film capacitor  $C_2$  decouples the offset at  $V_{OUT}$ . Note that if a more loosely controlled offset or high DC bias current device is used for U1 (such as a 5534), the simple biasing may not work as well. An alternate form of DC control is a servo loop for lowest output offset, using the general concepts described both in the microphone and RIAA preamp sections and the appendix. This tape EQ stage is topologically similar to the output stage of Figure 8.23, and could use a servo in a similar fashion.

It is not recommended that other op amps be substituted for the AD745 in this circuit, unless they are selected for low noise and distortion, for high gain, and for DC biasing compatibilities. Some alternatives which might be considered are the OP-37 or SSM-2139, which are bipolar. The most critical performance spec for U1 is low input noise, which in this application means both low voltage noise and low current noise. For high impedance heads, the current noise may well be more important than voltage noise, since the source impedance is inductive. To place this in

some perspective, a 1H head with a 1kHz Z of  $10\text{k}\Omega$  can have a effective 1kHz noise density component of  $10\text{nV}/\sqrt{\text{Hz}}$  due to the effect of amplifier noise current, when used with an  $1\text{pA}/\sqrt{\text{Hz}}$  amplifier. Of course, since noise sources add in root sum of squares fashion, in any given case there may be several noise sources which affect the equivalent input noise at the amplifier input. Reactive sources such as tape heads can require a low current noise amplifier, just as much as they also need one with low voltage noise. The AD745 excels in current noise, with a 1kHz noise density of  $6.9\text{fA}/\sqrt{\text{Hz}}$ . In contrast, low noise bipolar input amplifiers such as the OP-37 and SSM-2139 have noise current densities of  $0.4\text{--}0.6\text{pA}/\sqrt{\text{Hz}}$  (while their voltage noises are on a par with the AD745,  $\approx 3.5\text{nV}/\sqrt{\text{Hz}}$ ). For low-Z heads, an ultra-low

voltage noise device like the AD797 may be useful.

For highest circuit performance, use 1% metal-film resistors and 1-2% polypropylene film capacitors in the gain and equalization components, for the reasons noted in the RIAA discussions. Power supplies should be well regulated, and in the range of  $\pm 15\text{V}$  to  $\pm 18\text{V}$ .

While the above method of equalization can yield excellent results insofar as the *amplifier* frequency response is concerned, the tape head must also be properly terminated in the prescribed network for flattest playback response with a standard test tape.  $R_t$  and  $C_t$  are intended to serve part of this purpose, and final adjustments for frequency response may include trim of the EQ components.

**REFERENCES: TAPE PREAMPLIFIERS**

1. IEC, "Magnetic Tape Sound Recording & Reproducing Systems", Publication 94-1, Fourth Edition, 1981.
2. "Choosing and Using MRL Calibration Tapes", Magnetic Reference Laboratory, Inc., 229 Polaris Ave, Suite 4, Mountain View, CA, 94043.
3. Scott Wurcer, "Designing Circuits for Low Noise", discussion in AD745 data sheet, **Amplifier Reference Manual**, 1992, Analog Devices.
4. C. Motchenbacher, F. Fitchen, **Low-Noise Electronic Design**, Wiley, New York, 1973.

## AUDIO LINE LEVEL STAGES

Audio line level stages represent an intermediate level in dynamic range for practical audio circuits using modern IC devices. Line level amplifying stages generally work with single-ended or balanced input/output signal levels of 1-10V, and at medium levels of power. This section discusses some basic types of audio line stages which are:

■ *Line receivers* - including line receiver stages which accept single-ended or balanced line level signals with maximum noise immunity, and provide scaled outputs for further processing.

■ *Line amplifiers* - including amplifiers which scale a received signal in single-ended form and feature low distortion designs.

■ *Line drivers* - including single-ended and balanced drivers which are capable of driving appreciable output levels in terms of voltage swing, current levels, and/or difficult loads, such as capacitive lines.

Some general concepts of line driving and buffer amplifier design have been covered previously, with emphasis on video applications.<sup>[1-3]</sup> The material in this section continues the discussion and expands on those themes with

audio line-receivers and line-drivers as examples.

Audio transmission systems, unlike their video counterparts, do *not* generally use terminated transmission lines, so long transmission lines usually appear capacitive. Therefore, capacitive load isolation is important in audio drivers. In general, when building audio circuits of any type, "housekeeping" rules of layout and bypassing are strongly recommended, particularly for the buffer and line driver circuits.

The function of sending/receiving audio signals between various parts of a system has traditionally involved tradeoffs of one form or another. Fully differential or balanced transmission systems are best at rejecting low frequency and RF noise, so they are used for high performance, and are discussed in some detail following.

A typical audio system block diagram using differential transmission is shown in Figure 8.30. A balanced transmission system like this might use several input/output coupling schemes. Some major points distinguishing coupling methods are discussed briefly before considering actual circuits.



## BALANCED AUDIO TRANSMISSION SYSTEM

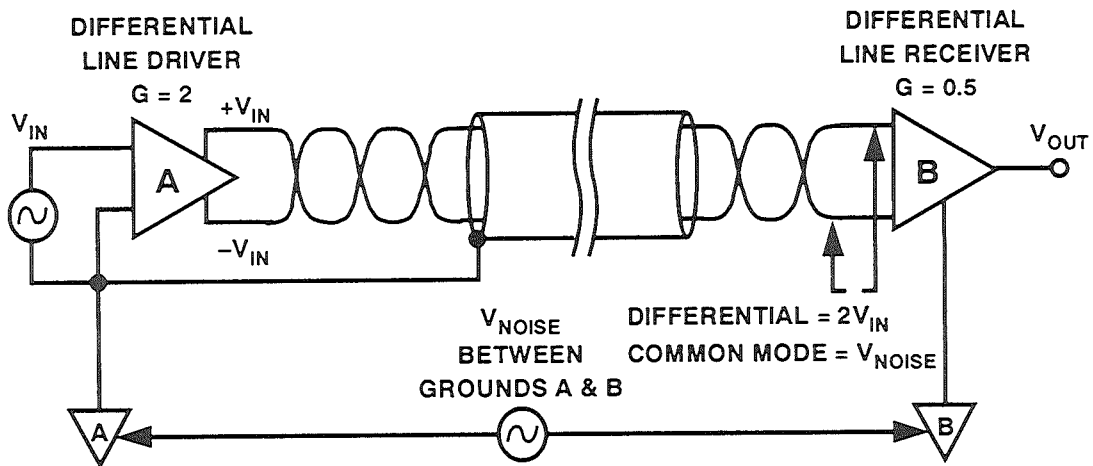


Figure 8.30

*Transformers*<sup>[4-7]</sup> have been a traditional audio line coupling element, at both input or output. They have well known problems with noise pickup, frequency response, distortion, and operating level. While these problems are all soluble to some extent, the solutions are usually costly. Nevertheless, transformers are unexcelled in some applications.

The outstanding virtue of transformers is the ability to *isolate*, which shows in two regards. They can galvanically isolate drive/receive stages (up to the breakdown potential of the windings), allowing signals to be transmitted across high ground potential differences (tens or hundreds of volts). This feature

is one quite difficult to achieve with solid state circuitry. Also, suitably designed transformers can have very high common mode rejection (CMR) in the audio range, in excess of 100dB. Some transformer-isolated driver stages are described in this section.

The general system of Figure 8.30 can in principle use either transformer or active coupling to the line. The goal for either approach is to reproduce a final signal  $V_{OUT}$  equal to  $V_{IN}$ , while rejecting noise between grounds A and B by 80- 100dB. A typical unity gain design uses a line drive of  $\pm V_{IN}$  and a receiver gain "G" of  $\frac{1}{2}$ , to maximize receiver CM range.

## AUDIO LINE RECEIVERS

Walt Jung, Adolfo Garcia

A brief review of the topologies and applications of audio line receivers helps us to understand their evolution. Figure 8.31 is a diagram of a classic 4 resistor differential amplifier. This circuit is also known as a simple form of

*instrumentation amplifier* (in-amp), which has evolved into today's modern IC instrumentation amplifiers.[8-12] Within audio applications, this and related circuits are usually known as "line receivers".

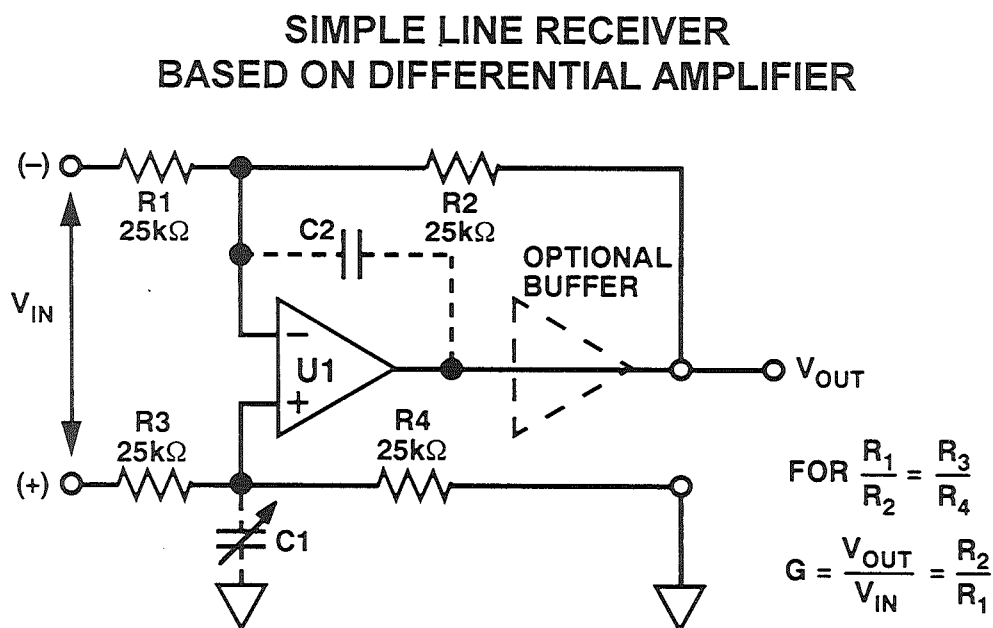


Figure 8.31

## The Simple Line Receiver

This simple line receiver circuit uses four resistors and an op amp for gain. Such bridge-based difference amplifiers are *critically* dependent upon the resistor ratio matching for good performance, an enormously important point. The amplifier can also be critical, but many practical limitations of these topologies arise from bridge *un*-balance which may be at AC or DC or both.

The circuit appears somewhat trivial, as the minimum ingredients are four matched film resistors and a good audio op amp. While this works functionally, how well it works in rejecting line noise is uncertain.

The main purpose of all line receivers is to reject common-mode noise, picked up on a twisted pair transmission line.

Even with a high quality op amp for U1, noise rejection is only as good as the resistor matching. More precisely, the *ratios* of resistors  $R_1/R_2$  and  $R_3/R_4$  must match extremely well to reject common mode noise (the absolute values are relatively unimportant).

0.1%, which will achieve a common mode rejection (CMR) of 66dB. If one resistor differs from the rest by 1%, the CMRR will drop to only 46dB. In general, the worst case CMR of a circuit of this type is<sup>[8]</sup>

Picking four 1% resistors from a single batch may yield ratio matching of

$$\text{CMR(dB)} = 20 \log \left( \frac{1 + R_2/R_1}{4K_r} \right) \quad \text{Eq. 8.20}$$

where " $K_r$ " is the *individual* resistor tolerance in fractional form, where 4 discrete resistors are used. A single component network with a net matching tolerance of  $K_r$  would probably be used for this circuit, in which case the expression would then be:

$$\text{CMR(dB)} = 20 \log \left( \frac{1 + R_2/R_1}{K_r} \right) \quad \text{Eq. 8.21}$$

Either case assumes a significantly higher *amplifier* CMR ( $\geq 100\text{dB}$ ).

Eq. 8.20 shows that the worst case CMR due to tolerance build-up for 4 unselected 1% resistors to be no better than 34dB. Clearly for high noise rejection, circuits such as these need four single-substrate resistors, with very high absolute and TC matching. Such networks using thick- and thin-film technology are available from companies such as Caddock and Vishay-Ohmtek, in ratio matches of 0.01% or better.

Some simulations may bring this point of critical matching home more clearly. Figure 8.32 shows the effect of various DC mismatches on a differential amplifier like that of Figure 8.31, with a single resistor mismatch in  $R_1$  of 0.1% (top trace), 0.01% (middle trace) and perfect matching (bottom). This display of CM error vs. frequency also shows a reactive imbalance for the perfect DC-balanced (bottom) case, due to an intentional capacitive mismatch.

# BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS DC TRIMS (SIMULATION)

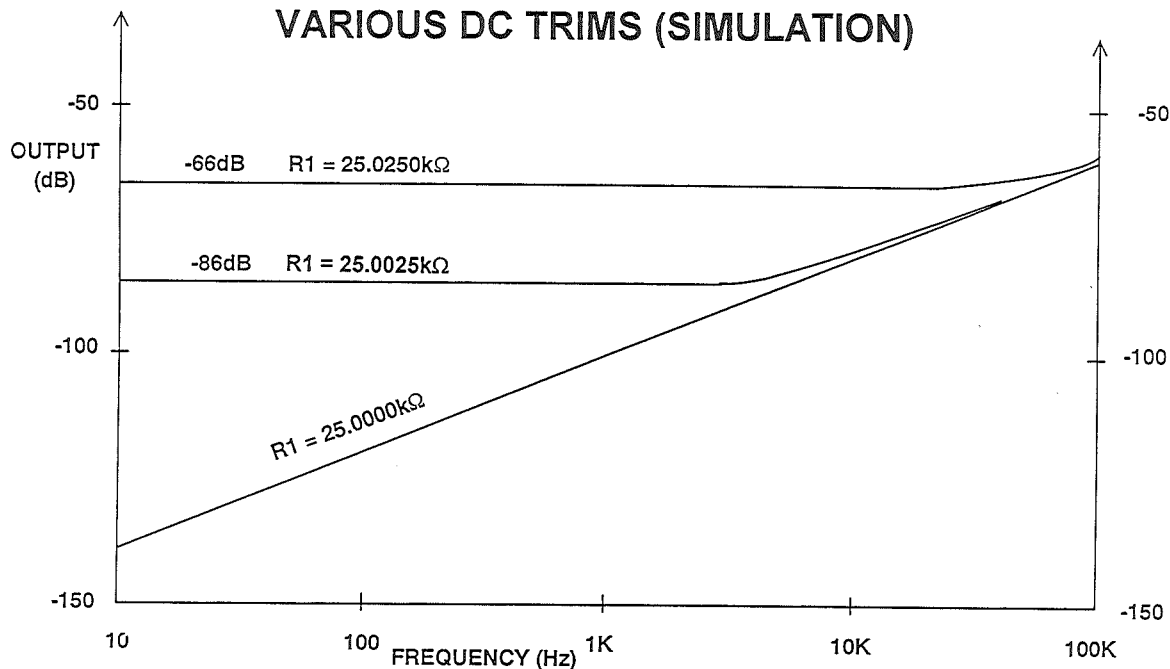


Figure 8.32

# BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS AC TRIMS (SIMULATION)

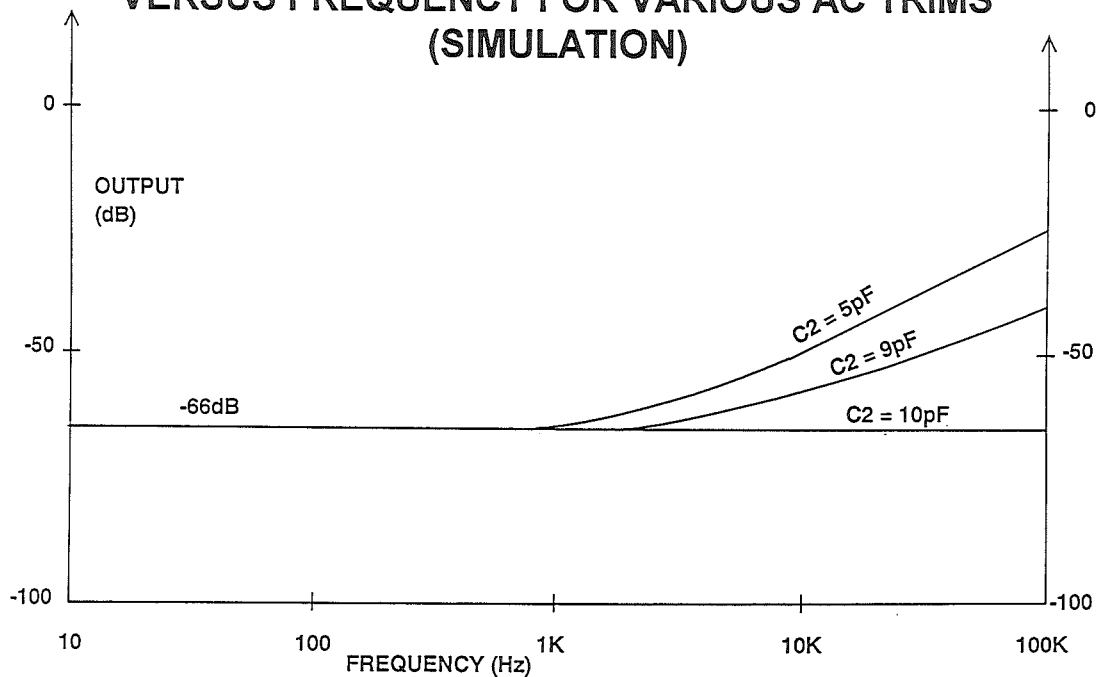


Figure 8.33

Figure 8.33 shows the effect of AC matching on this differential amplifier using 0.1% DC matched resistances, with  $C_2$  varied away from a nominal match to  $C_1$  (10pF). A 10% mismatch here results in a CM degradation as low as 10kHz.

Clearly, for wideband audio use, the bridge ratio needs to be maintained at AC as well as DC, to achieve flat CMR versus frequency. Capacitances from the  $R_2/R_1$  and  $R_4/R_3$  nodes need to be balanced. In practice, this is best achieved with very low and/or balanced parasitic capacitances at  $C_1$ - $C_2$ .

It is worthy of note that this circuit also has a highly desirable property; that is,

it *attenuates* the input CM voltage. Thus it inherently has some protection against overvoltage. In general, practical line receivers *require* input CM division, for safe use in harsh environments and to allow CM voltages to exceed the supply rails. For simplicity, the receiver gain resistors should also perform this function, as here.

The working CM input range of the circuit in Figure 8.31 is  $(1+(R_3/R_4)) \times V_{CM}(U1)$ , and the differential input resistance is  $R_1+R_3$ . Gain of the circuit may not easily be changed, because of the matched resistor ratios.

8

### Implementing the Simple Line Receiver Function

To present a reasonably high impedance to the line, receivers of this type typically use input resistances of 20k $\Omega$  or more. Given a well matched resistor network and low or balanced parasitic capacitances, suitable amplifiers for U1 are the AD711, AD744 and SSM-2131 (singles), and the AD712, AD746, OP-249, OP-275 and SSM-2139 (duals). With 10k $\Omega$ -25k $\Omega$  resistances, extremely low voltage noise in the amplifier is not highly critical, but high slew rate and output drive allows clean high frequency, high amplitude levels, and 600 $\Omega$  load capability. If low impedance loads need to be driven, output current of a standard op amp can be boosted with an “in-loop” unity gain buffer, connected between U1 and the load/feedback point. Devices such as the BUF-04 unity gain buffer or a follower-connected AD811 can serve for this function.

From the criteria of DC and AC trim/balance, the circuit in Figure 8.31 is most effective when the resistors and

amplifier are made in a single monolithic IC. The Analog Devices 8 pin SSM-2141 and SSM-2143 are such ICs, designed and characterized as low distortion, high CMR audio line receivers with net gains of unity (SSM-2141), and 0.5 (SSM-2143). The SSM-2141 has resistors just as shown in Figure 8.31, while the SSM-2143 uses 12k $\Omega$ /6k $\Omega$  resistors.

Even with these devices the resistor pinouts are such that buffers can be easily added if needed. In both the SSM-2141 and SSM-2143 for example, the amplifier output appears at pin 6, the feedback resistor is at pin 5, and the reference resistor is at pin 1. With  $V_{IN}(+)$  and  $V_{IN}(-)$  at pins 3 & 2, respectively, a unity-gain buffer can be connected as shown symbolically in Figure 8.31, and the buffered output taken from pin 5.

In applying circuits of the Figure 8.31 type (or other topologies which resistively load the source), a designer must

bear in mind that all *external* resistances added to the circuit can compromise CMR. To place this in perspective, a  $2.5\Omega$  or 0.01% mismatch can easily occur with wiring, and if not balanced

out, this mismatch will degrade the CMR of otherwise perfectly matched  $25k\Omega$  resistors to 86dB. These circuits are therefore best fed from balanced low impedance sources.

### Other Issues with the Simple Line Receiver

An application point which becomes relevant for large systems with multiple balanced pair lines is the issue of receiver *load balance*. Ideally, an audio line receiver should exhibit equal AC loading at the two inputs. With the simple line receiver of Figure 8.31, this goal is not met- i.e., the circuit does not present balanced loading to the input lines.

When driven with a balanced voltage  $2V_{IN}$ , as from complementary sources, the simple line receiver exhibits unbalanced input currents in the  $R_1$  and  $R_3$  legs, due to feedback action. For the values of Figure 8.31, the current in  $R_1$  is 3 times that in  $R_3$ .

In large systems with multiple balanced transmission line pairs, the current

imbalance in the input lines is potentially serious, as associated fields will not cancel as they do for balanced loading. There is thus potential for crosstalk in systems using simple line receivers.

But, while not optimum from a large system and/or line balance viewpoint, the simple line receiver is nevertheless quite useful in more modest situations. With resistors  $R_1$ - $R_3$  relatively high (20k or more), it is adequate for small-scale or confined systems where I/O lines are relatively short, few in number, or they are not cabled. In such uses, devices like the SSM-2141 and SSM-2143 serve well as efficient single IC receivers.

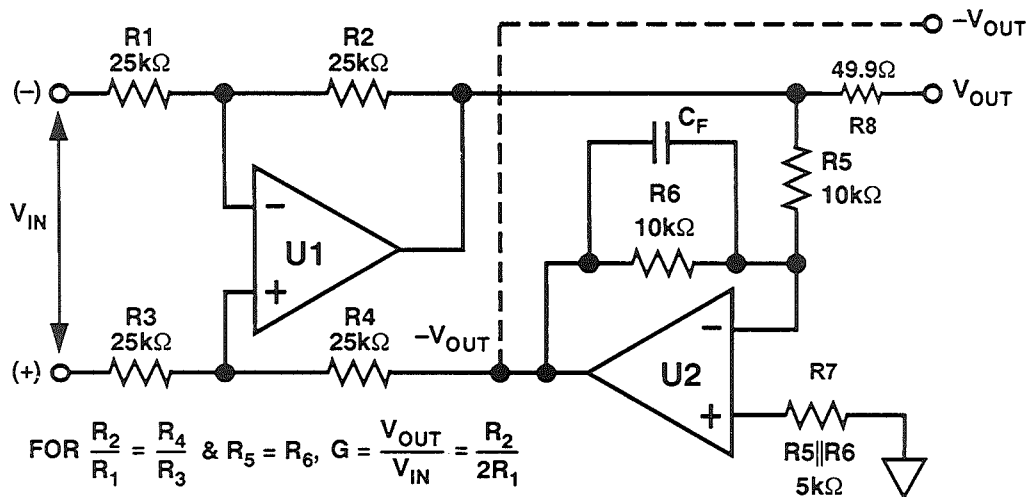
### Balanced Line Receivers

It is important in the highest performance systems that audio line receivers exhibit equal loading to the source at both inputs- i.e., they should be truly

balanced. At least two topologies behave in this way and are well suited for professional use in balanced systems.

Birtl<sup>[7]</sup> of the BBC has analyzed the simple line receiver topology and presented a modified and balanced form, shown in Figure 8.34. Here U1 uses an 4 resistor network identical to that of Figure 8.31, while feedback from unity

## BALANCED LINE RECEIVER USING PUSH-PULL FEEDBACK



Compared to Figure 8.31, and for like resistor ratios, the Figure 8.34 gain from  $V_{IN}$  to  $V_{OUT}$  is  $\frac{1}{2}$ , or a gain of -6dB (0.5) as shown. However it also offers an optional complementary output from U2,  $-V_{OUT}$ . Like the circuit in Figure 8.31, the gain of this circuit is not easily changed.

CM signals are seen by U1, and the CM range of the circuit is  $(1+(R_3/R_4)) \times V_{CM}(U1)$ . Differential input resistance is  $R_1+R_3$ .

8-57

### Alternate Balanced Line Receivers

Other types of instrumentation amplifiers can achieve fully balanced input loading, but may be undesirable for other reasons. For example, there are standard in-amp circuits which use either 2 or 3 amplifiers and have high input impedance, due to the use of non-inverting inputs.[8-11] The drawback of these circuits as line receivers lies in their limited gain and CM range, and

they also require four additional resistors for overload protection. Since these resistors also influence gain and CMR, they must be precision ratio matched types. As a net result, workable audio line receivers using such in-amps are not really practical as they require 8 or more matched resistors and 2 or 3 op amps.

### "All Inverting" Line Receiver

Figure 8.35 is an elegantly attractive topology which seems well suited to audio line receiver use. Using only inverting amplifiers, this circuit can be configured for very high CM voltage range and input resistance. With the resistor ratios matched as shown, the

CMR of this circuit can be better than that of the other circuits for a given resistor match, since neither amplifier sees CM voltage. The CM range of this circuit is  $(R_1/R_2) \times V_{OUT(MAX)U1}$ . The differential input resistance is  $R_1 + R_3$ .

### "ALL-INVERTING" LINE RECEIVER

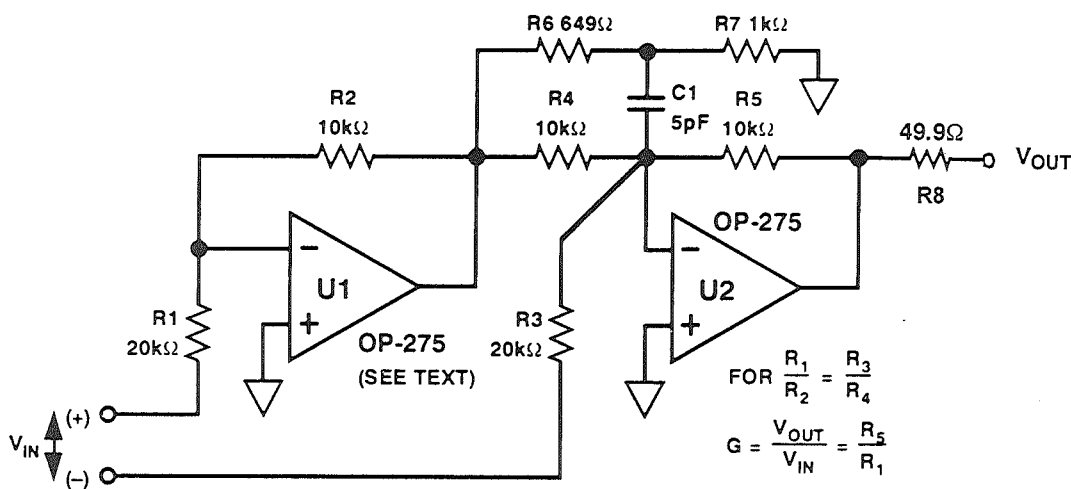


Figure 8.35



The circuit has the unusual and desirable property of single resistor gain adjustment via  $R_5$ , but *without* affecting CMR interaction. The gain extends from well below to well above unity. As shown it is driven with a balanced signal, but it can also be driven single-ended at either the (+) or (-) terminal, with no gain interaction from the opposite input port. A number of inputs can be summed, by adding additional ratio matched input resistor pairs (not shown). In this example the gain is set at 0.5, to be consistent with the general line receiver system requirements.

This circuit is also well known in its basic form.<sup>[8-11]</sup> However, in this example phase lead compensation is used to enhance high frequency CMR. A small capacitor shunting  $R_4$  with a value chosen to compensate for the gain-bandwidth of U1 compensates for the lag through U1, and maximizes phase matching of the  $\pm$  CM signals at U2. However, for op amps with gain bandwidths above a few MHz and practical resistor values, the capacitors required may be too small to be practical.

### Performance

The balanced line receiver configurations of Figure 8.34 and Figure 8.35 were tested for CM performance, with common conditions of  $G=0.5$ ,  $V_s=\pm 18V$ , and a 10Vrms input sweep, 20Hz-50kHz, filter bandwidth of 80kHz. The Figure 8.34 circuit was built with U1 as an SSM-2141, and U2 as an OP-275 inverter, with  $C_F=68pF$ . The Figure 8.35 topology was implemented with an OP-275 and a resistor network matched to 0.005%, with the phase lead network trimmed to the values shown (for best high frequency CMR). The results are shown in Figure 8.36.

Both circuits show excellent results, with  $\leq 1kHz$  CM errors of -100dB or less

The  $R_6$ - $R_7$ - $C_1$  tee network reduces the effective value of  $C_1$ , by dividing the applied voltage. A nominal division ratio for compensation capacitance ( $C_c$ ) can be approximated by:

$$K_c = \frac{1}{2\pi BW_{(U1)} R_4 C_1} \quad \text{Eq. 8.22}$$

where " $K_c$ " is the division ratio of  $R_6$ - $R_7$ . For this example, with  $BW(U1)$  about 5MHz (the closed loop bandwidth of U1),  $K_c$  is about 0.6, making  $C_c$  effectively about 3pF. Circuit parasitics, loading effects and part variations make this inexact; however, once nominal compensation for a given layout and devices is achieved, a 30dB CMR improvement in 10kHz CMR is possible relative to no phase compensation at all. While the phase compensation network is not absolutely necessary to the circuit's basic function, it does make a significant CMR performance difference for audio applications.

and little sensitivity to source impedances of 50 $\Omega$ -600 $\Omega$  (not shown). The circuit in Figure 8.35 offers better results at higher frequencies, perhaps due to the trimming technique used which is not applicable to the Figure 8.34 circuit. In the worst case, the CM errors are no worse than -80dB at 10kHz, very good for an untrimmed circuit. While CM performance data was measured for the Figure 8.35 circuit with several of the other dual devices mentioned with good- to-excellent results, the OP-275 was chosen to be illustrated here because of its generally higher output drive and all-around utility.

# BALANCED LINE RECEIVER COMMON MODE ERROR VERSUS FREQUENCY FOR $G = 0.5$ , $V_S = \pm 18V$ , $R_S = 600\Omega$

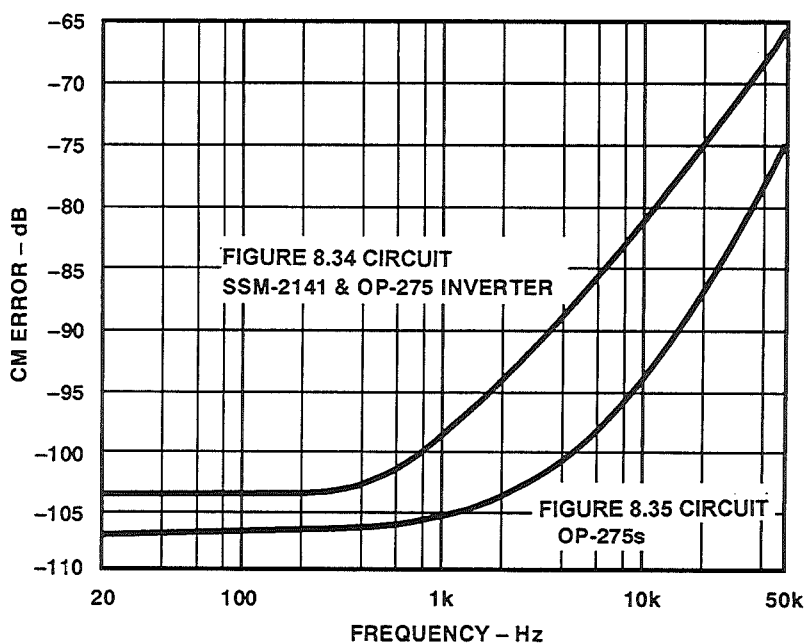


Figure 8.36

# BALANCED LINE RECEIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR $G = 0.5$ , $V_{in} = 1, 2, 5, 10V$ rms, $V_S = \pm 18V$

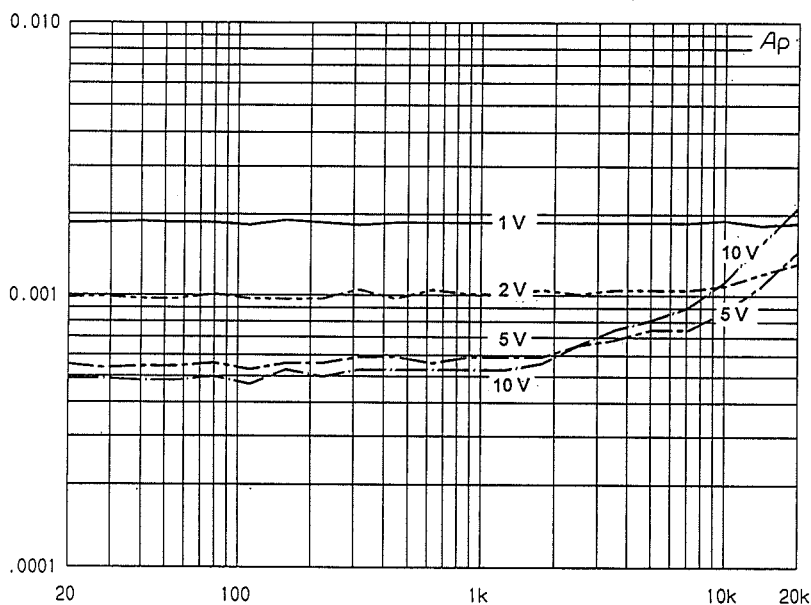


Figure 8.37

THD+N data was taken for both circuits and, while dominated by the noise floor at many levels, there are some differences worth noting between the two. Figure 8.37 shows THD+N performance of the Figure 8.34 SSM-2141/OP-275 circuit for loading conditions of 100k, and successive input sweeps of 1, 2, 5 and 10Vrms. The lower level sweeps are noise dominated, while the 5 and 10V sweeps show some increase in distortion at high frequencies. Distor-

tion in this circuit also rises with loading of 600 $\Omega$  (not shown).

The performance of the circuit in Figure 8.35 for similar drive conditions is shown in Figure 8.38, and for conditions of 600 $\Omega$  loading. These data indicate less loading and frequency dependence, due primarily to the OP-275's higher slewrate and greater output drive into 600 $\Omega$  loads.

**"ALL-INVERTING" LINE RECEIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $G = 0.5$ ,  $V_{in} = 1, 2, 5, 10V$  rms,  $V_S = \pm 18V$**

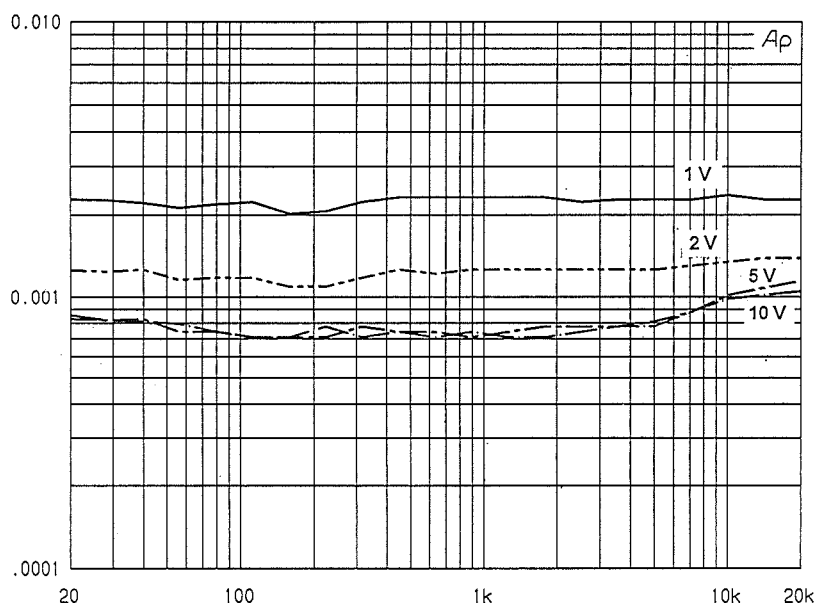


Figure 8.38

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## AUDIO LINE DRIVERS AND BUFFERS

Audio line drivers and buffer amplifiers can take a wide variety of forms, which include single-ended and differential output drivers, as well as transformer isolated drivers. Within these general formats there are many different performance options, many of which are covered in this section.

Many op amps useful as video drivers and buffers also do well as audio driv-

ers, because of the high current output stages necessary for good linearity over video bandwidths.<sup>[1,2]</sup> Some examples of video amplifiers which are useful for audio are the AD810, AD811, AD817, AD818, AD829, AD840 series, AD845, AD846, and AD847. Other types notable for either high or unusually linear output drives or other performance features useful in audio applications are the AD797, OP-275, and SSM-2131.

### High Current Buffer Basics

As a preliminary to detailed application discussions, some basic circuit principles germane to high current buffers and drivers should first be considered. With output currents up to 100mA or more, "housekeeping" details of bypassing, grounding and wiring become even

more important than usual, and must be considered. These are briefly discussed here in the context of high current buffers, using the unity gain buffer circuit of Figure 8.39 as a point of departure.

8

### UNITY GAIN STAND-ALONE BUFFERS

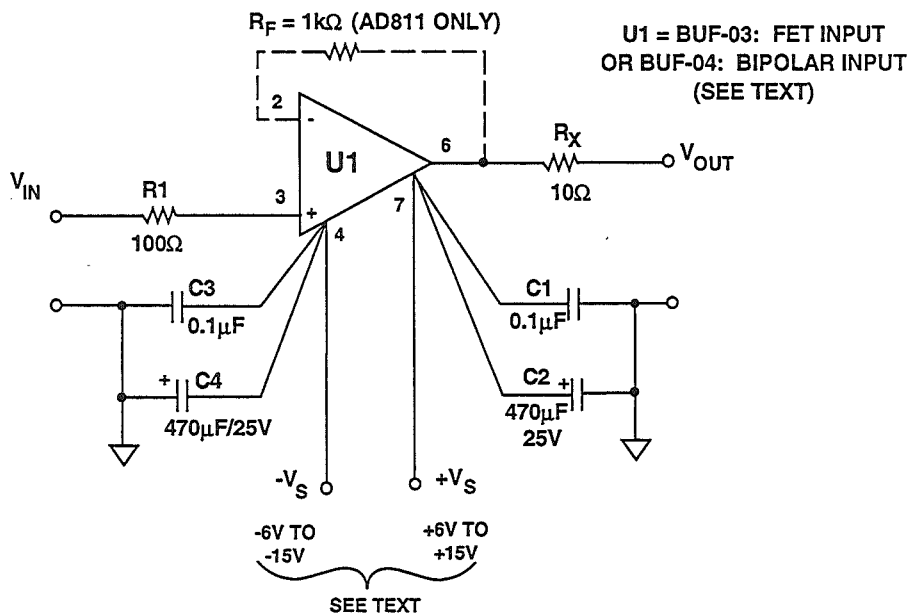


Figure 8.39

First, whichever IC is used for U1, close attention should be given to making buffer stages free from parasitic capacitances and inductances, at input, output, and supplies. Physical construction of buffer-drivers and other high current stages should be in accordance with high speed rules. A continuous copper ground plane is preferred, and circuit layout should be compact, with low capacitance around high-Z nodes. Signal and ground runs should be laid out with signal coupling and load current flow in mind.<sup>[3-6]</sup>

In addition, the power supplies should be well bypassed close to the high current supply pins. In Figure 8.39 this is indicated by the Kelvin connections of C<sub>1</sub>-C<sub>4</sub> to the  $\pm V$ s pins of U1. This should be standard practice for all high current stages, and must be used for all the driver applications in this section.

As a minimum, local low inductance/low ESR RF bypass caps should be used within 0.25" of the device supply pins, shown as C<sub>1</sub> and C<sub>3</sub>. These are preferably 0.1 $\mu$ F stacked polyester film low inductance type capacitors. For high peak current loads, the high frequency bypasses are paralleled by local, short lead/large value, low ESR electrolytics such as C<sub>2</sub> and C<sub>4</sub>, in a range of 470 $\mu$ F/25V and up. Note that capacitor ESR reduces in inverse proportion to electrical size and voltage rating, so larger size and/or voltage units help. These capacitors carry transient output currents, and should be aluminum electrolytic types rated for high frequency use, that is switching supply ones. Such capacitors tend to have low Q, and are thus less likely to cause power line resonances than are tantalum capacitors.

DC power management and dissipation are important with buffer ICs. For

example, the BUF-03 and the AD811 ICs can dissipate fairly large power levels even with light loading at supplies above  $\pm 12V$ , because the quiescent current of these devices is 15-18mA, relatively independent of operating voltage.

As a conservative rule of reliability, any IC with a power dissipation above 300mW should not be used without a heat sink. For buffer or driver circuits using more than 300mW, use the lowest thermal resistance package possible, and the appropriate heatsink (Thermalloy 2227 for the BUF-03 or other TO-99 ICs, or Aavid #5801 for the BUF-04, AD811 or other high dissipation 8 pin ICs).

Output resistor R<sub>X</sub> in this circuit should be 10 ohms or more, to isolate the buffer from capacitive loading (more on this, below). For an extra safety margin against possible de-stabilization due to capacitive loads, make this resistor as high as practical. Input resistor R<sub>1</sub> is a "bullet-proof" parasitic suppression device, and may be required for stability with some amplifiers but it is not absolutely essential for those we have discussed.

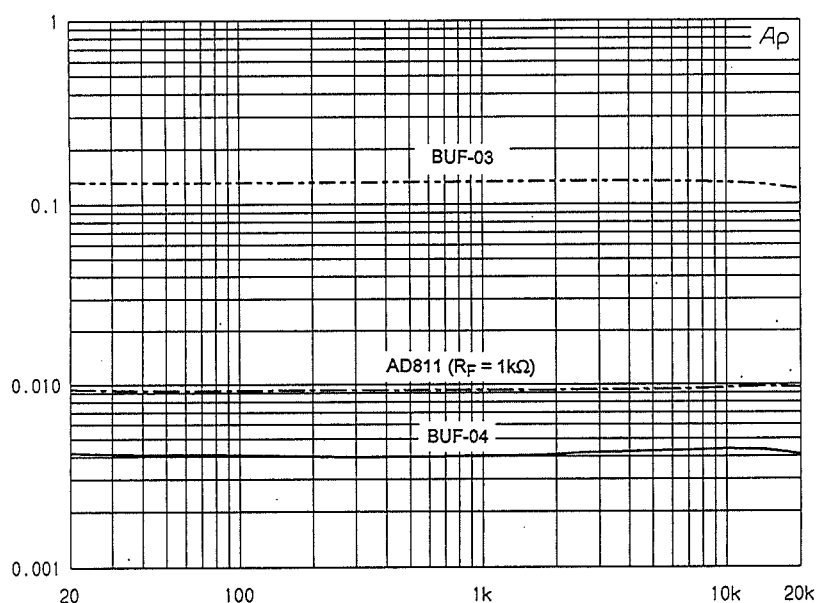
Because of this stage's very high bandwidth, low phase shift, and low output impedance, fast buffers such as this can be used both "stand alone" just as shown, and as a more conventional "in loop" buffer as well, to minimize loading of a weaker, slower amplifier. For any modest output amplifier this is an obvious improvement, as raises the linear output to more than  $\pm 100mA$  (with the AD811 or the BUF-04), while maximizing linearity, preserving gain, and lowering distortion.

Operating in a pure stand-alone mode, THD+N tests on several buffers are

shown in Figure 8.40, for conditions of 10Vrms into a 600Ω load. The BUF-03, a design with no closed loop feedback path, shows a distortion for these conditions of about 0.15%. The BUF-04, a closed loop transimpedance design buffer, shows a very low distortion of about 0.004%. The AD811 transimpedance amplifier, externally configured as a unity gain follower with

$R_F = 1k$ , shows an intermediate level of distortion, just under 0.01%. As a choice among these types, both the BUF-04 and AD811 are capable of more than  $\pm 100mA$  of output, and have input currents on the order of 1-2μA. The BUF-03 has a lower maximum output current ( $\pm 70mA$ ), but the advantage of an input current on the order of 200pA.

**VARIOUS UNITY-GAIN BUFFERS,  
THD + N (%) VERSUS FREQUENCY (Hz)  
FOR  $V_{out} = V_{in} = 10V$  rms,  $R_L = 600\Omega$ ,  $V_S = \pm 18V$**



**Figure 8.40**

### Capacitive Loading

Audio output/input stages are typically operated as voltage source drivers feeding high impedance loads. When connected with long transmission lines between stages, the result is that the driver sees an unterminated line, which can appear highly capacitive.

Audio driver stability with capacitive loading is not always easy to achieve.

Fortunately, some standard techniques exist for stabilizing op amp drivers with capacitive loads, and these can be implemented in a reasonably direct fashion.

A good rule for any type of audio driver is that capacitive loading should be expected in any application, however benign it may seem. Signal trace ca-

capacitance can build up quickly, even on the same PC board, and particularly for long signal runs. "Off board" circuits at the end of short cable runs should be evaluated for capacitive loading much more carefully, with the capacitive loading characterized as well as pos-

sible. "Outside world" drivers where load capacitance is either poorly defined or undefined must be considered a worst case, and bullet-proofed accordingly with appropriate design techniques.

### Overcompensation

Overcompensation of an op amp to achieve stability inadvisable with audio circuits, as it compromises both slew rate and bandwidth. Furthermore, few audio op amps provide the compensation pins to allow such overcompensa-

tion (some exceptions to this are the 5534, the AD829, and the AD744). In some situations overcompensation may be useful, but generally other techniques for dealing with capacitive loads are more effective.

### Passive Capacitive Load Compensation

A passive form of capacitive load compensation is the most simple and practical for general purpose audio circuits. Shown in Figure 8.41, this circuit stabilizes an amplifier output against capacitive load by isolating it with a series resistor,  $R_X$ . The amplifier feedback loop is *passively* buffered from capacitive load effects by  $R_X$ , and amplifier stability is maintained. The series resistor  $R_X$  does cause a voltage drop proportional to load current, so for low impedance loads it must necessarily be low. Typical  $R_X$  values will lie in the range of 10-50 $\Omega$ , which produce small but (usually) manageable power losses for loads of 500 $\Omega$  or more.

Obviously, the choice of U1 buffer amplifier must be consistent with the load requirements, and generally the ability to drive high currents is an

advantage. The AD845 is shown in this example, and is chosen for its minimum gain of 100kV/V driving 500 $\Omega$  or higher loads, output currents of up to  $\pm 50$ mA, and a slew rate of 100V/ $\mu$ s. In addition, it has a cascode FET input stage with low bias current, and low distortion.

For low impedance loads,  $R_X$  at 50 $\Omega$  produces a 10% gain error and a similar power loss. Gain accuracy also suffers, if the load is remote or its impedance is not known accurately.

If the load  $R_L$  is known and stable, then adding gain resistors  $R_F$  and  $R_{IN}$  can compensate for the gain loss caused by  $R_X$ . For this unity gain driver, when these resistors are matched in ratio to  $R_X/R_L$ , a nominal overall gain of 1 is restored.



## PASSIVE CAPACITIVE LOAD ISOLATION USING ISOLATION RESISTOR, $R_X$

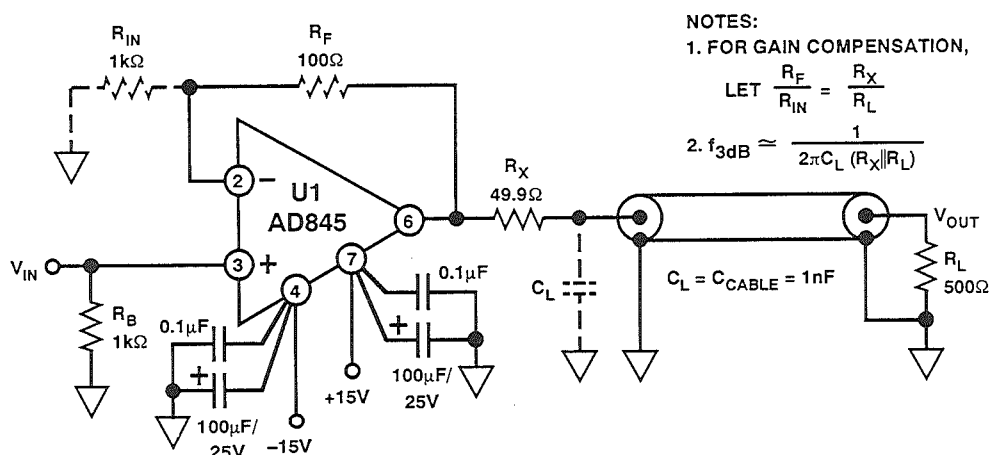


Figure 8.41

This capacitive load compensation technique is quite simple and can be effective, but it does have drawbacks. Already mentioned is loss of gain (or gain accuracy) and loss of output power, there is also loss of bandwidth for high values of load capacitance, and a possible loss of slew rate. For example, while the AD845 has a basic slew rate of  $100V/\mu s$ , this falls to  $50V/\mu s$  with  $C_L = 1nF$ . In general the slew rate in this circuit will be limited to  $I_o(max)/C_L$  V/s, when this figure is

*smaller* than the intrinsic device slew rate (as is the case here).

The technique of Figure 8.41 is a general one, and is useful with any amplifier. High speed, high current devices will of course make best use of it for audio. The applications following show op amps generally suited for line driving use by virtue of their unusually high current output, low output resistance, and/or speed capabilities.

## Internal Capacitive Load Compensation

An even simpler method of driving capacitive loads is to use an op amp which has an *internal* load compensation network. This is an amplifier design feature that makes capacitive loading virtually transparent to the user. It is used in a number of ADI op amps, including the AD817, the AD829, and the AD847.

As the simplified AD817 schematic in Figure 8.42 shows, part of the amplifier compensation network is capacitor  $C_F$ , which is connected in a feedforward fashion around the unity gain output

stage. Under normal circuit operation with low capacitive loads this network is bootstrapped by the output stage, little voltage appears across it, and it has little effect on the output. With capacitive loading and large signals, current is drawn from the output stage, which causes a voltage drop across the  $C_F$  network and a corresponding current in it. This adds additional compensation capacitance to the amplifier's internal compensation node, slowing down the amplifier and keeping it stable.

### AD817 SCHEMATIC ILLUSTRATING INTERNAL CAPACITIVE LOAD COMPENSATION

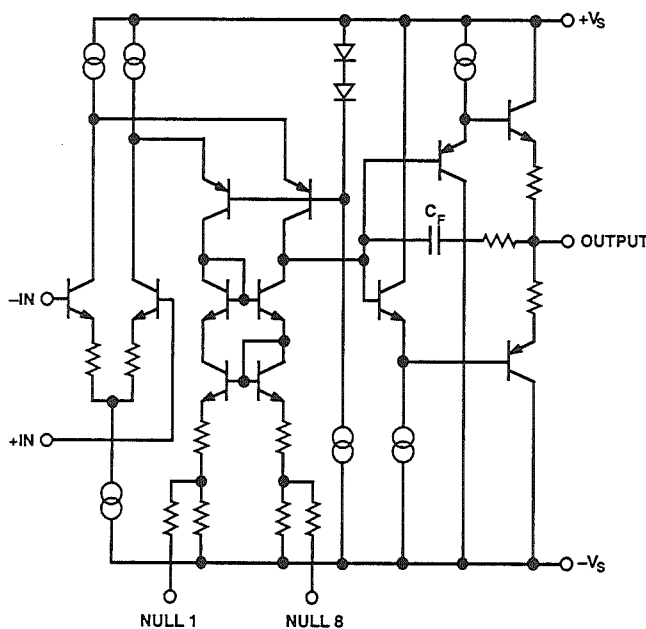


Figure 8.42

Like the passive form of capacitive load compensation, internal compensation causes in loss of bandwidth and slew rate. In addition it is signal dependent,

having greater effect with large signals than small ones. It can also cause some distortion, since the amplifier bandwidth varies dynamically.

### External "In Loop" Capacitive Load Compensation

External *in loop* compensation is the most flexible and accurate of the compensation techniques available for capacitive load isolation. It is flexible because it can, in principle, be applied to any unity gain stable op amp, whether it is operating in inverting or non-inverting mode. It is accurate because it includes the isolation resistance  $R_X$  within a DC feedback loop. This feature makes the low frequency gain accuracy as good as the resistors used (assuming adequate gain in the op amp). Its main problem is that it re-

duces bandwidth and slew rate, like the other techniques we have discussed.

The basic circuit illustrating operation is shown in Figure 8.43. It is a non-inverting stage with a gain of 2, where resistor  $R_X$  isolates the capacitive load  $C_L$ . While the circuit is similar to that in Figure 8.41, the resistive feedback is taken from the *load* side of  $R_X$ , automatically compensating for gain errors and loading. The basic gain expression is similar to that of a standard non-inverting op amp stage.

8

### CAPACITIVE LOAD ISOLATION USING "IN-LOOP" COMPENSATION

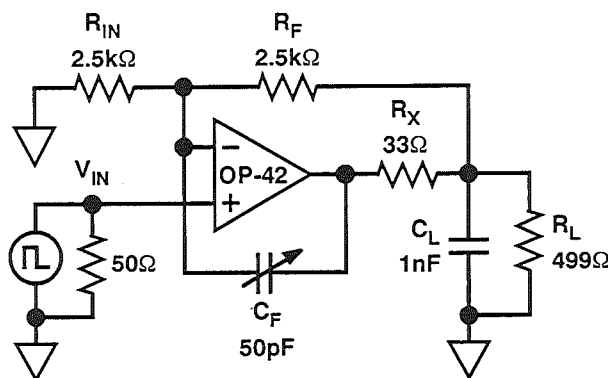


Figure 8.43

The capacitor  $C_F$  provides compensation for the additional lag introduced by  $C_L$ .  $C_F$  can be adjusted to cancel the effect of  $C_L$  and provide a well damped step response. This counters the ten-

dency towards overshoot, ringing or oscillation caused by  $C_L$ , but it does not allow maximum bandwidth, as the closed loop bandwidth of the stage is still a function of  $R_X$  and  $C_L$ .

The value chosen for  $R_X$  is not critical, and the stage can be tuned with values in the range of 10-100 $\Omega$ .  $R_X$  should not be excessively large, as this will degrade power output as well as bandwidth.

The optimum value for  $C_F$  is a function of  $R_X$ ,  $C_L$  and the gain resistors, and with fixed values for  $R_F$ ,  $R_{IN}$  and  $R_X$ , will track  $C_L$ . While several references suggest procedures for predicting  $C_F$ ,<sup>[7,8]</sup> the best practical approach is to select a close nominal value for  $C_F$ ,

then adjust it for optimum pulse response *in the final circuit layout*.<sup>[9]</sup> This approach takes additional parasitic capacitances into account.

Low values of  $R_F/R_{IN}$  minimize sensitivity to stray capacitance. This will force  $C_F$  higher than 20pF and into a range of greater predictability and stability.  $C_F$  is best a composite of an NPO capacitor in parallel with an NPO trimmer. Alternately, it can be a single fixed value, once the optimum value has been verified in final layout.

### Op Amp Device/Topology Related Distortions

Single-ended audio drivers can be built using Figure 8.41 as a starting point, and that circuit, with appropriate choice of op amp and gain can well serve as a basic audio driver. The non-inverting gain stage architecture is preferable for a line driver, since it loads the signal source less, and it does not invert. However, this configuration is subject to certain distortions, which should be understood in order to obtain the best performance in an application.

The test circuit in Figure 8.44 loads the amplifier with 500 $\Omega$  and 1nF. Such a load is quite difficult to drive, so this test is useful for discovering the behavior of devices under adverse load conditions. By programming a gain of 2 the test ensures the presence of sufficient common-mode voltage to test for common-mode related distortion as well. The tests are conducted with  $\pm 18$  V

supplies and an analyzer bandwidth of 10 Hz-80kHz. We find that amplifiers with linear output stages and high drive capability may still exhibit non-linearity in this test, due to the non-linear C/V characteristics of the amplifier inputs. The effect can be minimized by matching the source impedances at +In and -In, which reduces the differential component of this error.

This point is illustrated by Figure 8.45, a family of plots for the OP-275 op amp tested in the circuit of Figure 8.44, using various values of source resistance  $R_S$ . Distortion is lowest when  $R_S$  is equal to the parallel equivalent of  $R_F$  and  $R_{IN}$ , (about 910 $\Omega$ ). For higher or lower values of  $R_S$ , distortion rises. Appreciably higher source impedance (10k $\Omega$ ) can cause the distortion to occur at lower frequencies, making performance much worse overall.

## TEST CIRCUIT FOR LINE DRIVER AMPLIFIERS

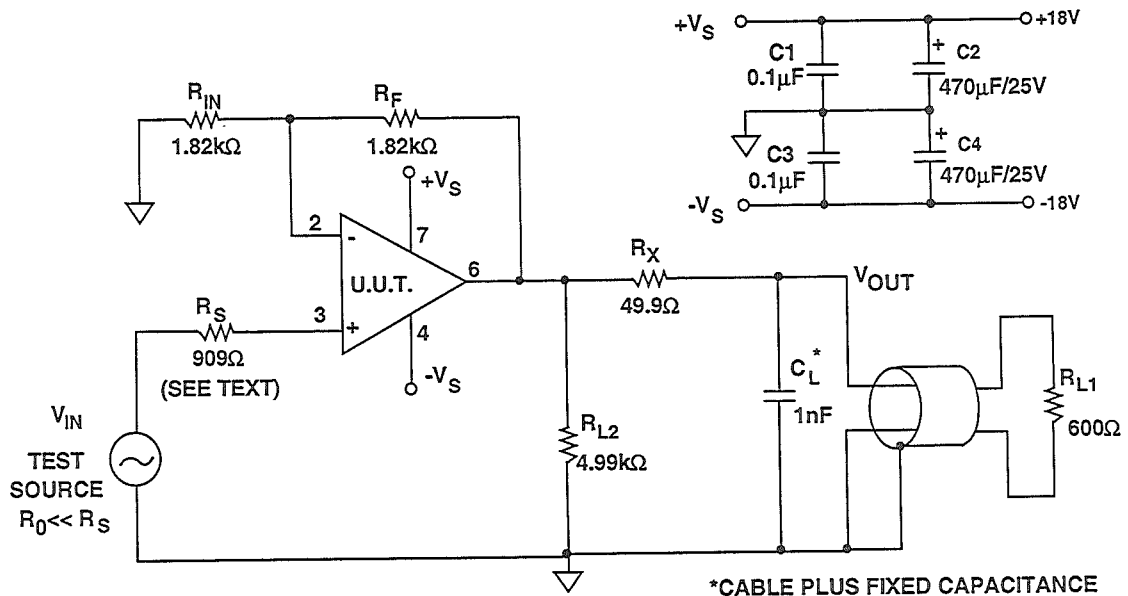


Figure 8.44

**FOLLOWER MODE  $R_S$  SENSITIVITY: OP-275**  
**THD + N (%) VERSUS FREQUENCY (Hz) FOR**  
 $V_{out} = 7V$  rms,  $R_S = 910\Omega$ ,  $100\Omega$ ,  $10k\Omega$ ,  $R_L = 500\Omega$ ,  $V_S = \pm 18V$

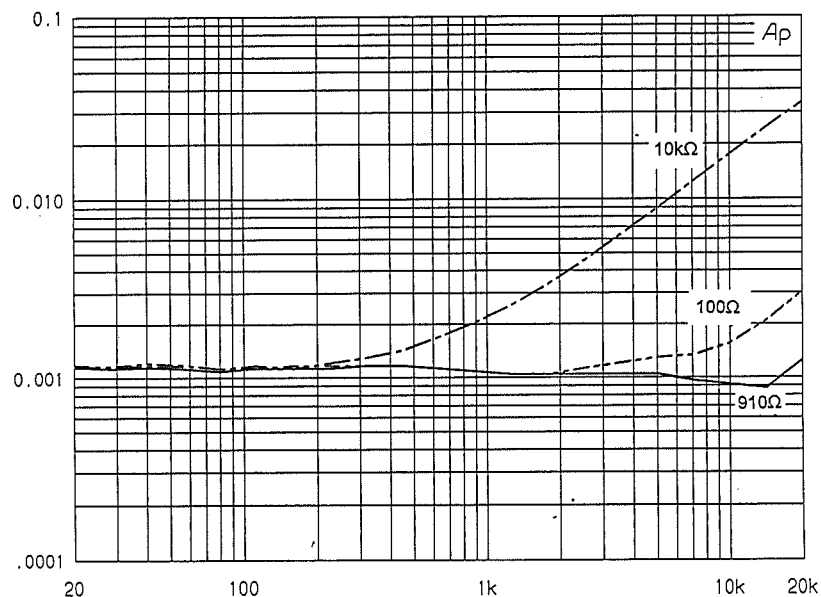


Figure 8.45

Whenever possible, amplifiers which operate as voltage followers should have their source impedances balanced for lowest distortion. The OP-275 device is but one example, and its sensitivity to CM distortion effects is not at all unique. Most solid-state amplifiers (op-amps, in-amps, and discrete bipolar transistors and FETs) are subject to nonlinear C/V effects to some extent. In the tests of other amplifiers,  $R_s$  was maintained at  $910\Omega$  to minimize the effects of this distortion mechanism.

With high output, high slew rate linear amplifiers, the distortion generated for

these test conditions can be comparable to the distortion of the test equipment (Figure 8.46). Here the AD817, AD818 and AD845 amplifiers show THD+N which is essentially equal to the residual distortion of the measurement system for these conditions, and appreciably below 0.001%.

Amplifier types expressly designed for audio use do well in these THD+N tests, (Figure 8.47). The industry standard 5534 is near or just above the residual level, the OP-275 plot falls just above 0.001%, and the 5532 is slightly higher.

**SET "A" DRIVERS, THD + N (%) VERSUS FREQUENCY (Hz)  
FOR  $V_{out} = 7V$  rms,  $R_s = 909\Omega$ ,  $R_L = 500\Omega$ ,  $V_S = \pm 18V$**

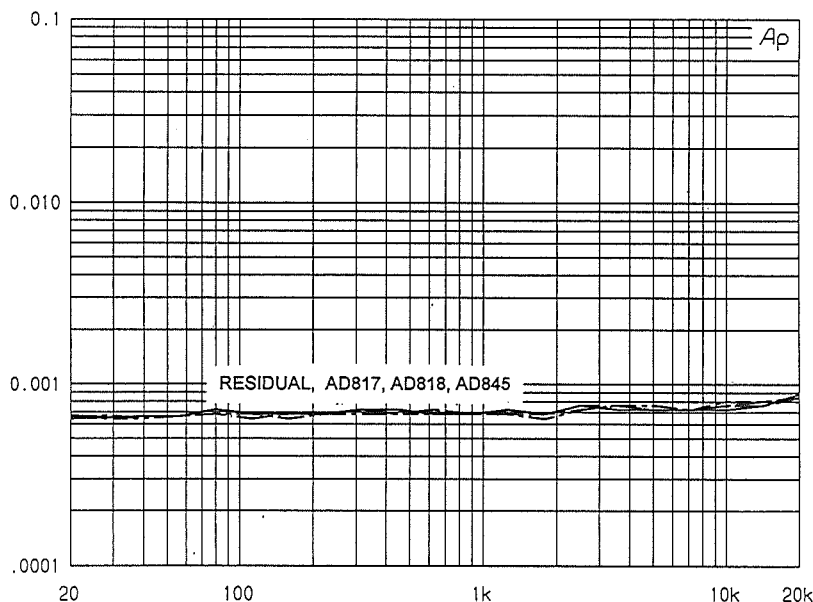
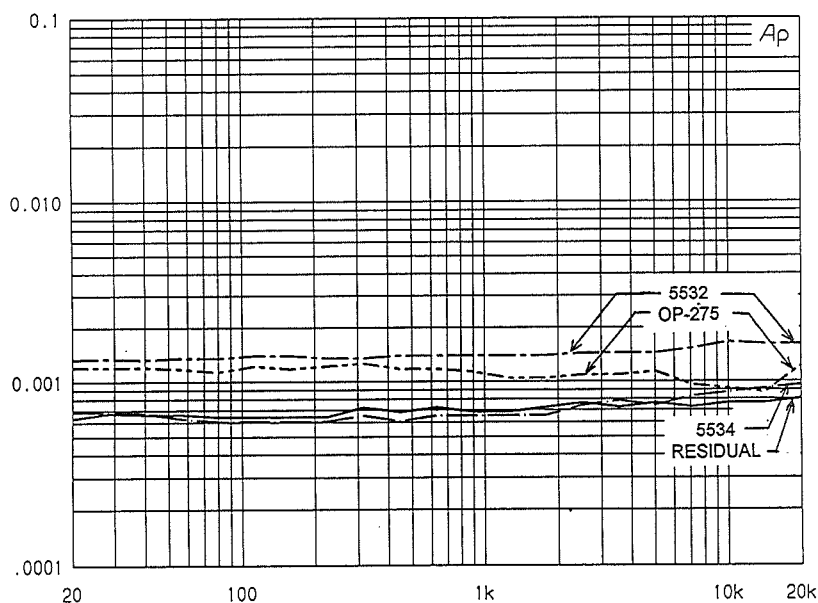


Figure 8.46

**SET "B" DRIVERS THD + N (%) VERSUS FREQUENCY (Hz)  
FOR  $V_{out} = 7V_{rms}$ ,  $R_S = 909\Omega$ ,  $R_L = 500\Omega$ ,  $V_S = \pm 18V$**



**Figure 8.47**

## SINGLE-ENDED LINE DRIVERS

This section discusses a variety of line drivers which drive single-ended lines,

optimized for different environments.

### Consumer Equipment Line Driver

One common driver application is a line output stage for consumer preamps, CD players, etc. This is an economical stage with a nominal gain of 5 to 10 times operating from supplies of  $\pm 10V$  to  $\pm 18V$ , with a rated output of 2-3V<sub>rms</sub> driving loads of 10k $\Omega$  or more. For

simplicity of biasing and minimum output DC offset, AC coupling is used, and the circuit is often fed from a volume control. Such a stage is shown in Figure 8.48, using an OP-275 op amp as the gain element.

## CONSUMER EQUIPMENT LINE DRIVER

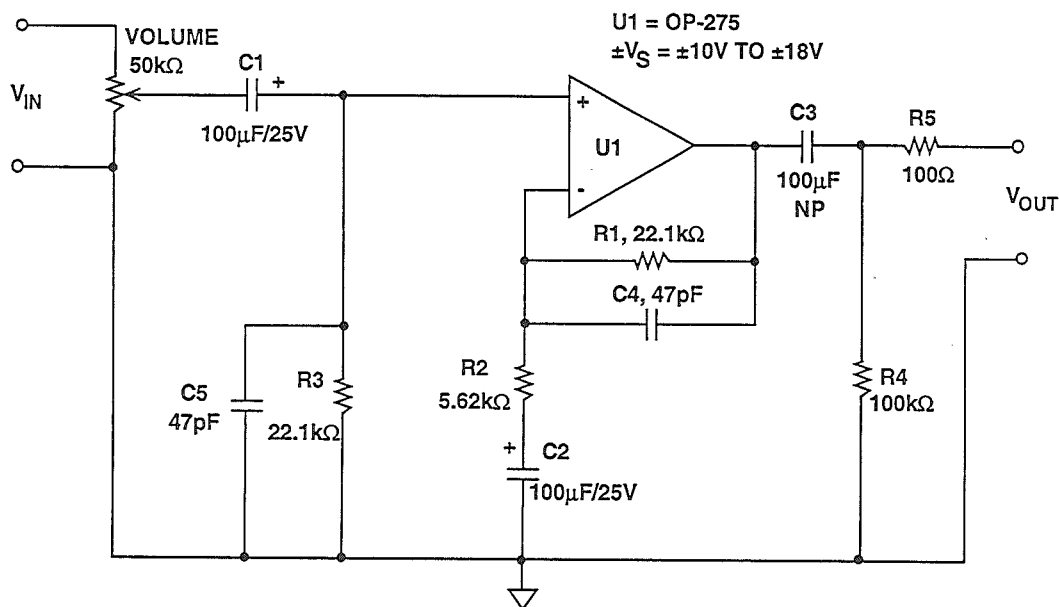


Figure 8.48

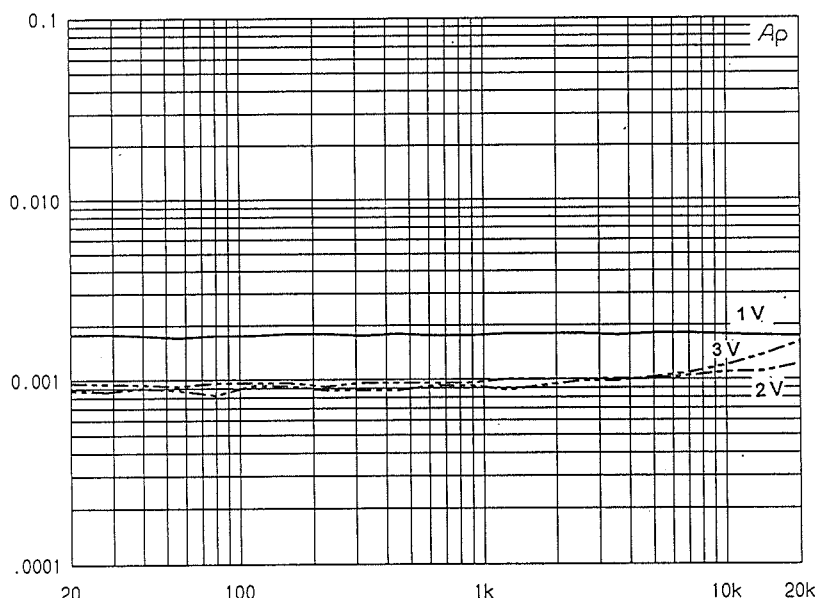
In this circuit input and feedback resistors  $R_1$  and  $R_3$  are made equal, so the nominal DC bias at  $U_1$ 's output is zero. The  $U_1$  bias current flowing in these resistors polarizes coupling capacitors  $C_1$  and  $C_2$ . The OP-275 has PNP input transistors, so this bias is positive. If the OP-275 is replaced with an amplifier with NPN input transistors, the polarity will be reversed and the polarity of  $C_1$  and  $C_2$  should also be reversed.  $R_1$  and  $R_2$  set the stage gain (nominally 5).  $R_2$  and  $C_2$  set the LF rolloff at 0.3 Hz. This allows the gain to be increased by reducing  $R_2$  without changing  $C_2$ . The output capacitor,  $C_3$ , must be non-polar, since the output offset may be of either polarity. If the

output can tolerate a DC offset of  $\pm 10$  mV (max - typical value is  $\pm 2.5$  mV),  $C_3$  may be omitted.

THD+N performance of the stage is shown in Figure 8.49 for outputs of 1, 2, and 3Vrms into a 10k $\Omega$ /600pF load, using  $\pm 18V$  supplies with an  $R_S$  of 1k $\Omega$ . At lower output levels performance is noise limited, while at a 3V output level there is a slight increase in high frequency distortion. Although this application is an example of a circuit where the amplifier source impedances cannot be perfectly matched (due to variations of the volume control), performance is still good.



**CONSUMER EQUIPMENT LINE DRIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 3V$  rms,  $R_L = 10k\Omega/600pF$ ,  $V_s = \pm 18V$**



**Figure 8.49**

Noise is the limiting factor for lower level signals, and if lower noise is required,  $R_2$  can be reduced. The practical limit to noise is the volume control's finite output resistance which causes higher noise at high output resistance, because of interaction with the noise current from U1. If the effective  $R_s$  at the volume control is  $10k\Omega$ , a  $1.2pA/\sqrt{Hz}$  noise current from U1 will

produce an input referred  $12nV/\sqrt{Hz}$  noise voltage.

The driver stage of Figure 8.48 is flexible, and also operates at supplies as low as  $\pm 10V$  with outputs up to  $3V_{rms}$ , with a slight distortion increase. At  $\pm 5V$ , outputs up to  $2V_{rms}$  are possible, but with distortion still higher but remaining  $\leq 0.01\%$ .

### Paralleled Output Line Driver

Often a modest increase in output may be needed from a driver, but circumstances may not warrant the use of an additional buffer. Figure 8.50 shows how the second section of a dual op amp can be used to provide additional load drive. In this circuit, the U1A section is an  $\times 5$  voltage amplifier, while U1B is a voltage follower, used simply to provide

additional current to the load. Current sharing between the amplifier stages is determined by output resistors  $R_4$  and  $R_5$ , and the composite stage drives  $600\Omega$  loads with lower distortion than a single OP-275 section. THD+N data is shown in Figure 8.51 operating from  $\pm 18V$  supplies, and for output levels of 1, 2, 5, and  $9V_{rms}$  into  $600\Omega$ .

## PARALLELED OUTPUT LINE DRIVER

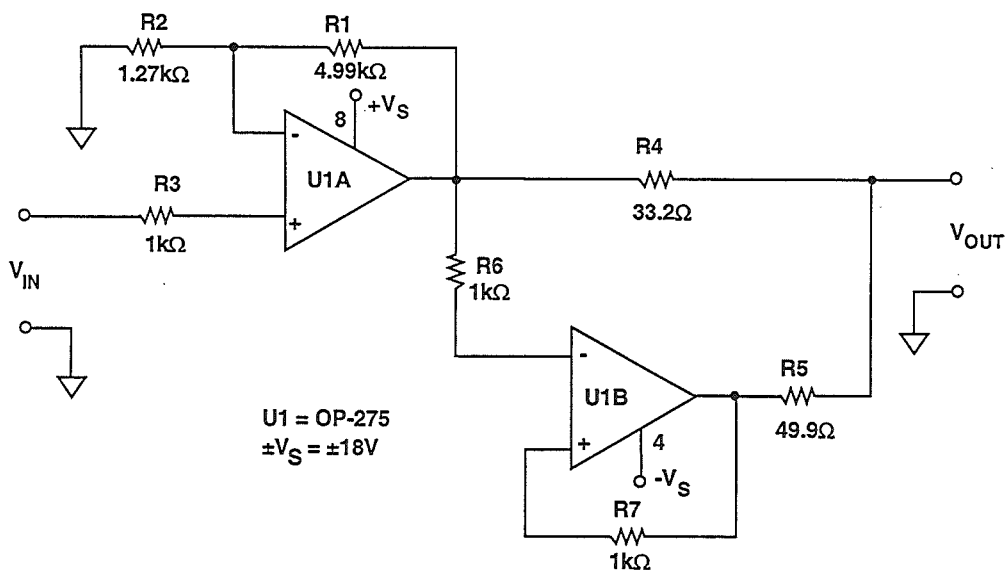


Figure 8.50

**PARALLELED OUTPUT LINE DRIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 5, 9V$  rms,  $R_L = 600\Omega$ ,  $V_S = \pm 18V$**

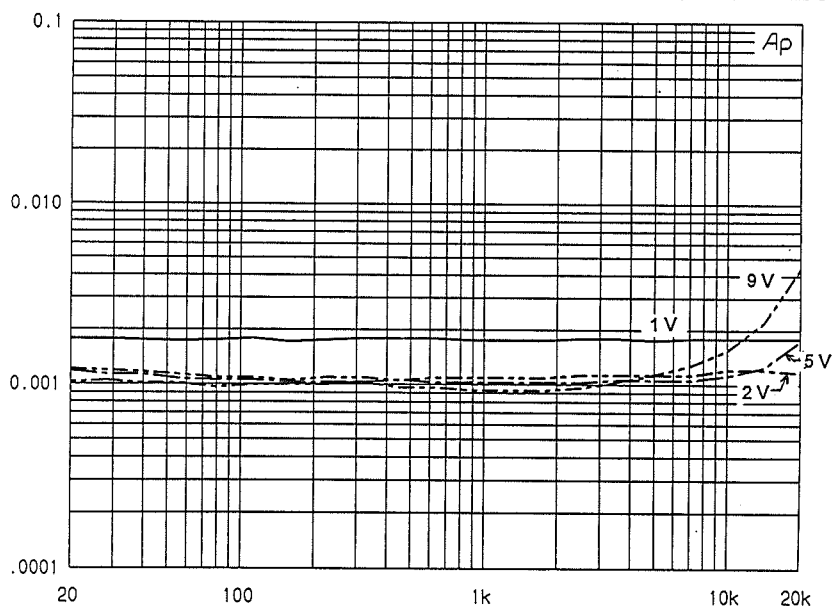


Figure 8.51

This scheme can be used with any unity gain stable dual op amp and various gain levels. For different devices and

gains the ratio of  $R_4$  and  $R_5$  may need adjustment for lowest distortion into the load.

### A WIDE DYNAMIC RANGE ULTRA LOW DISTORTION DRIVER

Single-ended line drivers may seem simple, but when both high dynamic range and low noise and distortion are necessary, it is difficult to choose a suitable amplifier.

The AD797 has very low input noise of  $<1 \text{ nV}/\sqrt{\text{Hz}}$  and a distortion cancelling output stage, and is exceptionally well-suited to line driver applications.<sup>[11]</sup>

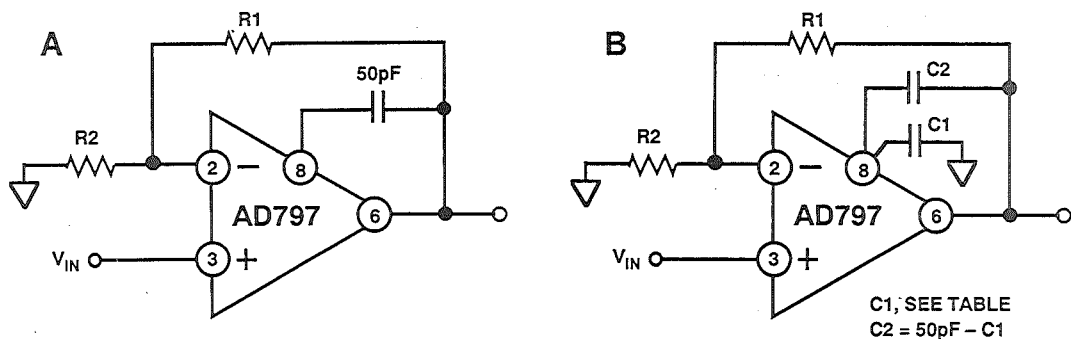
The AD797 has a single voltage gain stage, which consists of a folded cascode input and a bootstrapped (and therefore very high impedance) current mirror load. The combination has a gain of about 146 dB. Using a single stage

allows improvements in bandwidth, phase margin, settling time, and noise over more conventional two-stage op-amps.

The AD797 is used like any other 5 pin op amp (Figure 8.52). Low values for gain resistors  $R_1$ - $R_2$  are recommended for best noise, and selecting these resistors should be done with care, as values  $\geq 100\Omega$  will limit noise performance. Suggested values for gains of 10-1000 times are noted in the "A/B" column of the table in Figure 8.52. The AD797 can drive loads of up to 50mA, and is specified for distortion when driving loads of  $600\Omega$ .

8

### AD797 RECOMMENDED CONNECTIONS FOR DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT



	A / B		A			B		
	R1	R2	C1	C2	3dB	C1	C2	3dB
	$\Omega$	$\Omega$	pF	pF	BW	pF	pF	BW
G=10	909	100	0	50	6 MHz	0	50	6 MHz
G=100	1k	10	0	50	1 MHz	15	33	1.5 MHz
G=1000	10k	10	0	50	110 kHz	33	15	450 kHz

Figure 8.52

For amplifier applications requiring the best possible distortion, the capacitors  $C_1$  and  $C_2$  should be used. The single 50 pF capacitor,  $C_2$ , in Figure 8.52A compensates for output stage distortion without affecting forward gain.

At higher gains a second capacitor,  $C_1$ , from the compensation node to ground, enhances open-loop bandwidth and improves high frequency performance by "decompensating" the amplifier and increasing its gain-bandwidth product (Figure 8.52B). The effects of  $C_2$ , and  $C_1$  and  $C_2$ , are summarized in the table.

A family of distortion curves for various AD797 gain configurations driving  $600\Omega$  is shown in Figure 8.53. At low frequencies the noise is far greater than the distortion, which cannot be measured. At high frequencies distortion is measurable, but still extremely low. The distortion for a gain of 10 times at 20kHz for example, is  $\approx 0.0001\%$ , implying a dynamic range of 120dB referenced to  $3V_{rms}$ , and even more at higher level signals.

### TOTAL HARMONIC DISTORTION (THD) VERSUS FREQUENCY @ 3V rms FOR AD797 DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT CIRCUIT

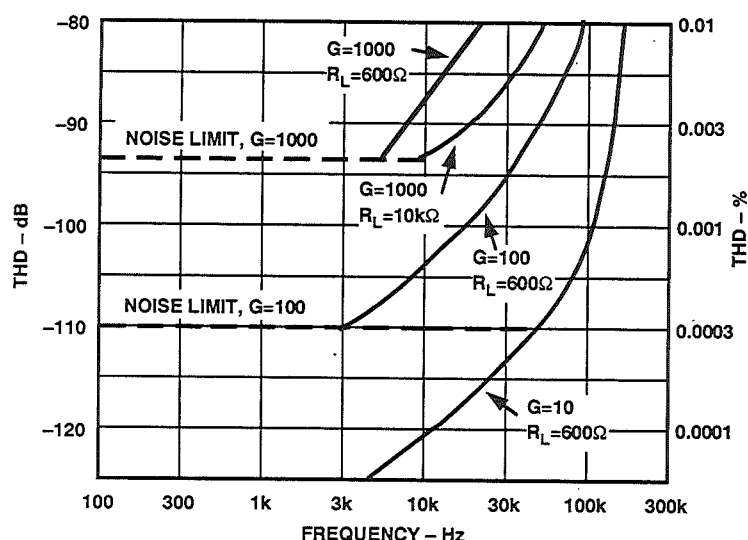


Figure 8.53

## Current Boosted Line Drivers

When a driver must drive loads of less than  $600\ \Omega$ , it is unlikely that an op-amp can handle the task unaided. In such cases a current-boosted design allows loads down to  $150\ \Omega$ .

Figure 8.54 is an example of a high quality current boosted driver. It uses an AD845 as a gain stage and voltage driver, and a unity gain current booster. The overall voltage gain is  $\times 5$ , but may easily be modified by  $R_1/R_2$ . For lowest CM distortion,  $R_3$  is set equal to  $R_1 \parallel R_2$ .

The amplifier used for U2 may be either the AD811 op amp, or the BUF-04 buffer. The AD811 op amp is configured as a follower, with  $R_5$  connected as shown. The BUF-04 is internally con-

nected as a follower. In either case, both the U1 and U2 devices *must* have a heat sink, and be used with supplies of  $\pm 17\text{V}$  or less. As usual, the power supplies must be well bypassed.

For loads of  $150\ \Omega$ , the series isolation resistor  $R_4$  is only to  $22.1\ \Omega$ , to minimize power loss and to allow levels of  $7\text{V}_{\text{rms}}$  or more. The THD+N data for this circuit is shown in Figure 8.55 and Figure 8.56 respectively, using the AD811 and BUF-04 as the U2 buffer. The test conditions are successive input sweeps resulting in 1, 2, 4 and  $8\text{V}_{\text{rms}}$  out. The test power supplies are exactly  $\pm 18\text{V}$ . *Production versions of this circuit, where the power supplies will be less accurately defined, should use nominal supplies no greater than  $\pm 17\text{V}$ .*

## CURRENT BOOSTED LINE DRIVER

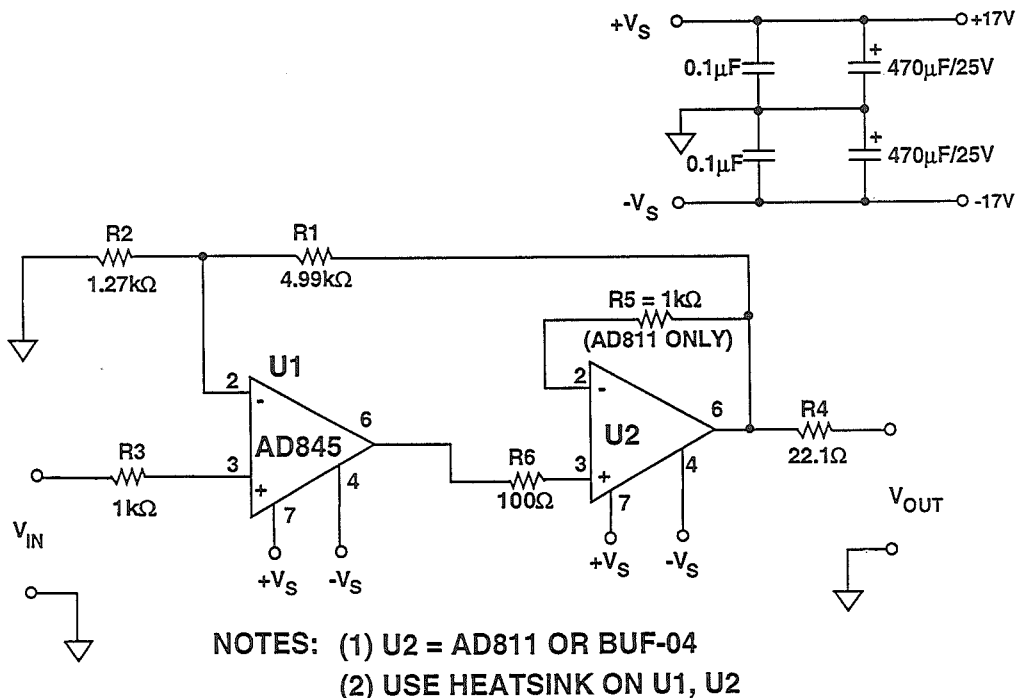


Figure 8.54

**CURRENT BOOSTED DRIVER USING AD811**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 4, 8V$  rms,  $R_L = 150\Omega$ ,  $V_S = \pm 18V$**

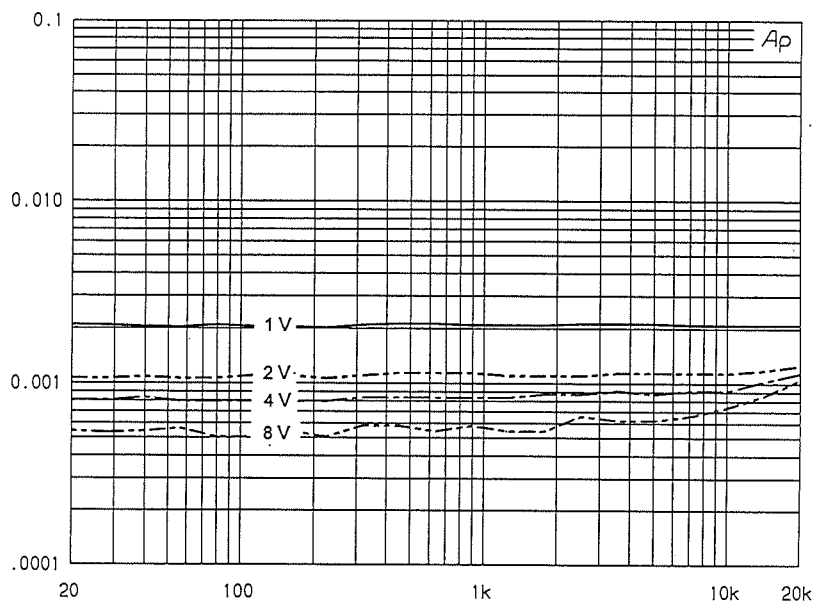


Figure 8.55

**CURRENT BOOSTED DRIVER USING BUF-04**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 4, 8V$  rms,  $R_L = 150\Omega$ ,  $V_S = \pm 18V$**

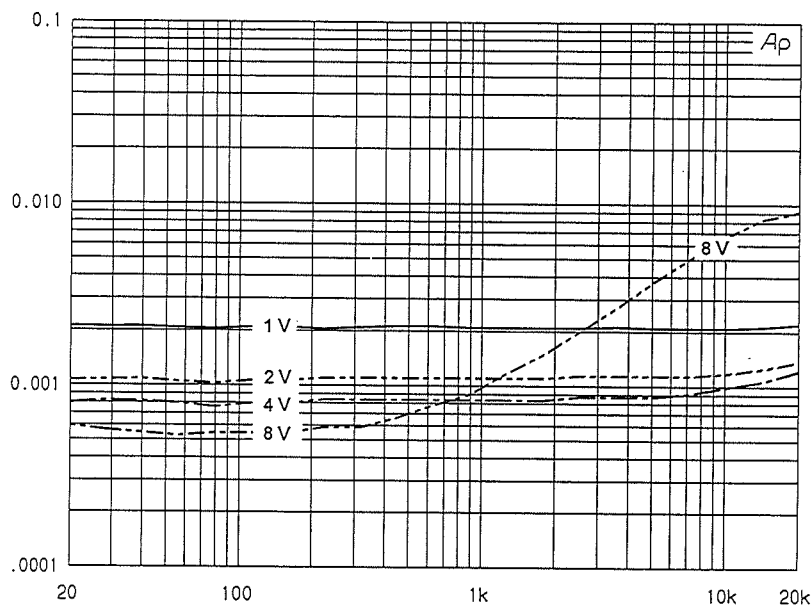


Figure 8.56

For the AD811 buffer, the data of Figure 8.55 shows THD+N dominated by noise and residual distortion at nearly all levels and frequencies while driving 150Ω. A very slight rise in distortion is noted above 10kHz, yet it is still  $\approx 0.001\%$ . The BUF-04 (Figure 8.56) is nearly as good at low output levels, but shows some distortion increase at the 8Vrms output at higher frequencies.

There is a tradeoff involved in the choice between these two devices. The

BUF-04 has a standby dissipation of about 300mW, while the AD811 has nearly double this dissipation, 560mW. So while the AD811 yields lower distortion, it must be operated more conservatively. Only the minimum supply voltage required to sustain a given output should be used.

Variants of this circuit technique will be found in later parts of this section in other driver applications.

### A Composite Current Boosted Driver

Another useful current-boosted circuit technique combines the best features of two different amplifiers into a single composite structure, producing a very high performance line driver.<sup>[12,13]</sup> With an FET input IC as the input stage, there is no noticeable dc offset change from source resistance variations of a typical volume control, allowing dc coupling. A high current, wide band current booster output stage drives line impedances down to 150Ω with excellent linearity.

A composite amplifier allows the best features of two dissimilar ICs to be exploited. Figure 8.57 shows a low distortion composite amplifier using two amplifier ICs.

A factor which aids performance is that U1 operates unloaded, and the compensation pin (5) drives U2. This removes possible U1 output stage distortion. The overall gain bandwidth and slew rate of U1 are boosted by the voltage gain of

U2, an AD811. The AD811 is used for its  $\pm 150\text{mA}(\text{max})$  output current.

The circuit has an overall gain of 5, set by  $R_1$  and  $R_2$ . The gain of the output stage, which is set by  $R_3$  and  $R_4$ , should be

$$\left[ \frac{\text{Overall Gain}}{2} - 1 \right]$$

As the AD811 is a transimpedance amplifier, there is an optimum value for  $R_3$ , which should be used, and the gain varied with  $R_4$ . Further design details are available in Reference 12.

The composite amplifier performance is remarkable for its modest complexity. For a typical audio load of 600Ω, THD+N at output levels of 1, 2, 4 and 8Vrms is shown in Figure 8.58. Distortion is only visible above the noise at the higher frequencies. The circuit will drive low impedance loads down to 150Ω. At supply voltages above  $\pm 12\text{V}$ , U2 requires a heat sink.

## COMPOSITE CURRENT BOOSTED LINE AMPLIFIER

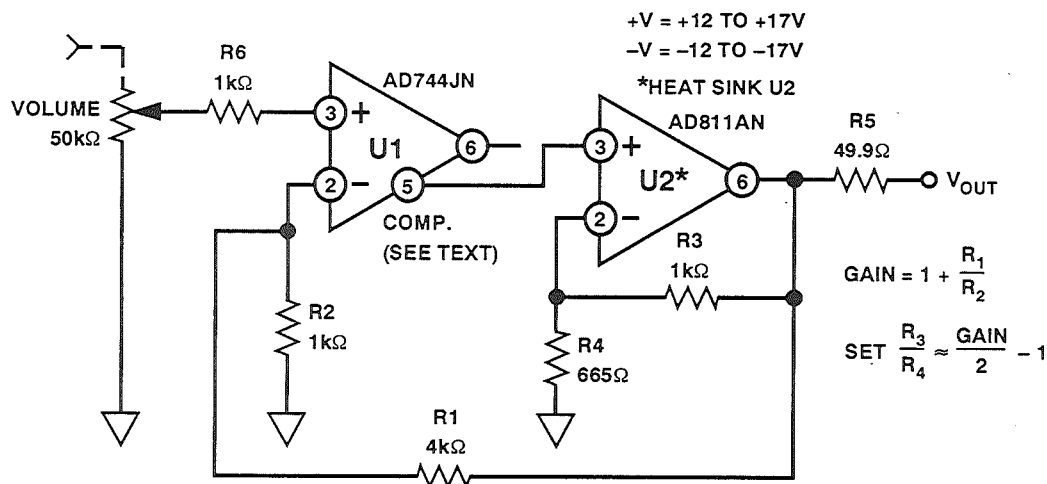


Figure 8.57

## COMPOSITE CURRENT BOOSTED DRIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR V<sub>out</sub> = 1, 2, 4, 8V rms, R<sub>L</sub> = 600Ω, V<sub>S</sub> = ±18V

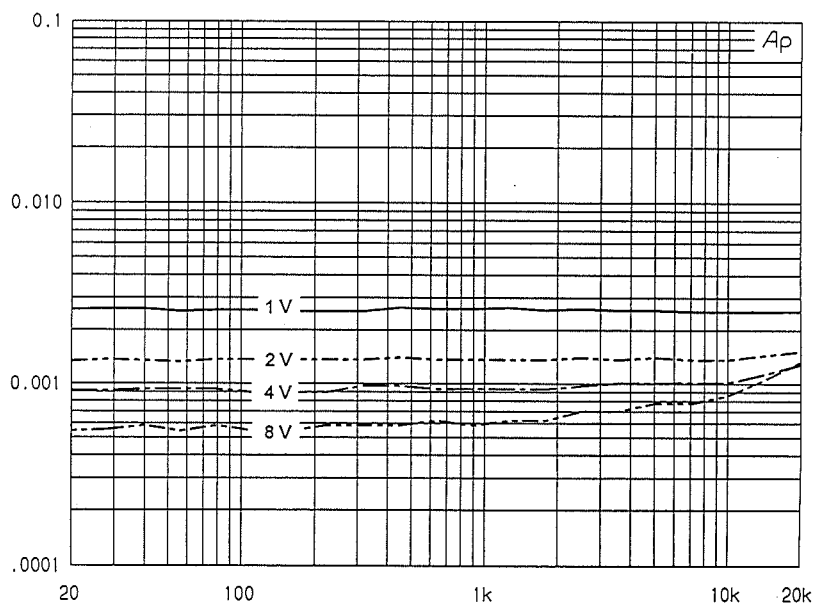


Figure 8.58



## Differential Line Drivers

Standard circuits for line drivers are not nearly as well-defined as standard circuits for line receivers. This section

discusses a variety of possible circuits, varying greatly in complexity and performance.

### “Inverter-Follower” Differential Line Driver

A straightforward approach to developing a differential drive signal of  $2V_{IN}$  is to amplify in complementary fashion a single-ended input  $V_{IN}$ , with equal gain inverter/follower op amps. With op amp gains of  $\pm 1$ , this develops outputs  $-V_{IN}$  and  $+V_{IN}$  with respect to common, or  $V_{OUT} = 2V_{IN}$  differentially.  $V_{OUT}$  can be scaled further, but gains  $< \pm 1$  are less practical.

OP-275 and one 8x20k film resistor network (Figure 8.59). Here U1A provides the gain of -1, while U1B operates at a gain of +1. The differential output signal across the balanced output line is  $2V_{IN}$ , and the differential output impedance is equal to  $R_A + R_B$ , or  $100\Omega$ .

This “inverter/follower” driver is easily built with a dual op amp such as the

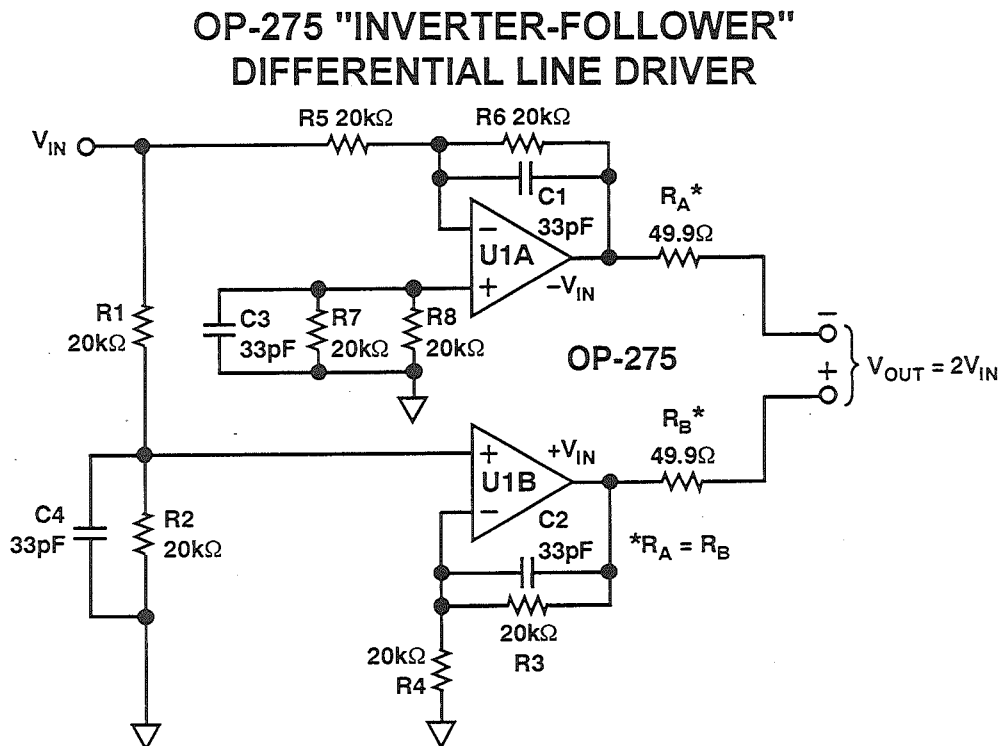


Figure 8.59

Use of similar values for gain resistors around the two amplifiers matches the channel noise gains, and makes the network easy to obtain. It also matches the source impedances seen by the op amp inputs. Capacitors  $C_1$ - $C_2$  provide HF rolloff, and enhance stability when driving capacitive lines. This circuit has high performance for its cost and simplicity. If a resistor network is used for

$R_1$ - $R_7$ , it can be built with only 6 components.

THD+N performance of this circuit is shown in Figure 8.60. The distortion is about 0.001%, and somewhat higher at 1V output level (noise limited). Maximum output level is about 12Vrms into 600 $\Omega$  before clipping.

**OP-275 "INVERTER-FOLLOWER" DIFFERENTIAL DRIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 5, 10V$  rms,  $R_L = 600\Omega$ ,  $V_S = \pm 18V$**

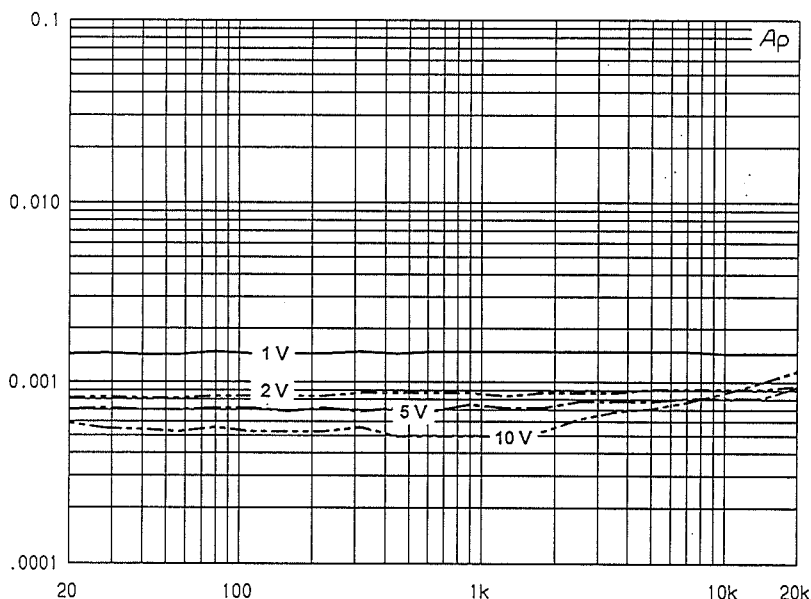


Figure 8.60

This type of differential line driver can run into application problems, and should be used with some care. The driver circuit uses two single-ended drivers, and they produce output signals with respect to the source ( $V_{IN}$ ) common point.

If the receiver used with this driver has a high impedance differential input (such as those discussed in the line receiver section) there is no real problem. However, one side of the differential output from Figure 8.59 *cannot be grounded without side effect*. This is

because the source drive  $V_{OUT}$  is *not* floating.

In this sense, the circuit is *pseudo differential*, and it should not be used indiscriminately. Nevertheless, within small and well defined systems, it has

the obvious advantage of simplicity and can achieve high performance. With the matched sources  $R_A$  and  $R_B$  of  $49.9\Omega$  there will be no damage even if one output is shorted, but half the signal will be lost.

### Cross-Coupled Differential Line Driver

A more sophisticated form of differential line driver uses a pair of *cross-coupled* op amps with both positive and negative feedback paths. The general form of this type of circuit is a cross-coupled *Howland* circuit, named after the inventor of the classic resistor bridge current pump. The cross-coupled form was described by Pontis in a solid-state transformer emulator for high performance instrumentation.<sup>[14]</sup>

This configuration provides maximum flexibility, allowing a differential output

signal  $V_{OUT}$  to be maintained independent of the load common connections. This means that either side can be shorted to common, as with a transformer.

Figure 8.61 shows the SSM-2142 balanced line driver IC use. The SSM-2142 consists of two cross-coupled Howland circuits, plus an input buffer. The trimmed multiple resistor array and three op amps are packaged in an 8 pin miniDIP IC.

8

### SSM-2142 CROSS-COUPLED DIFFERENTIAL LINE DRIVER USED IN BALANCED DRIVER / RECEIVER SYSTEM

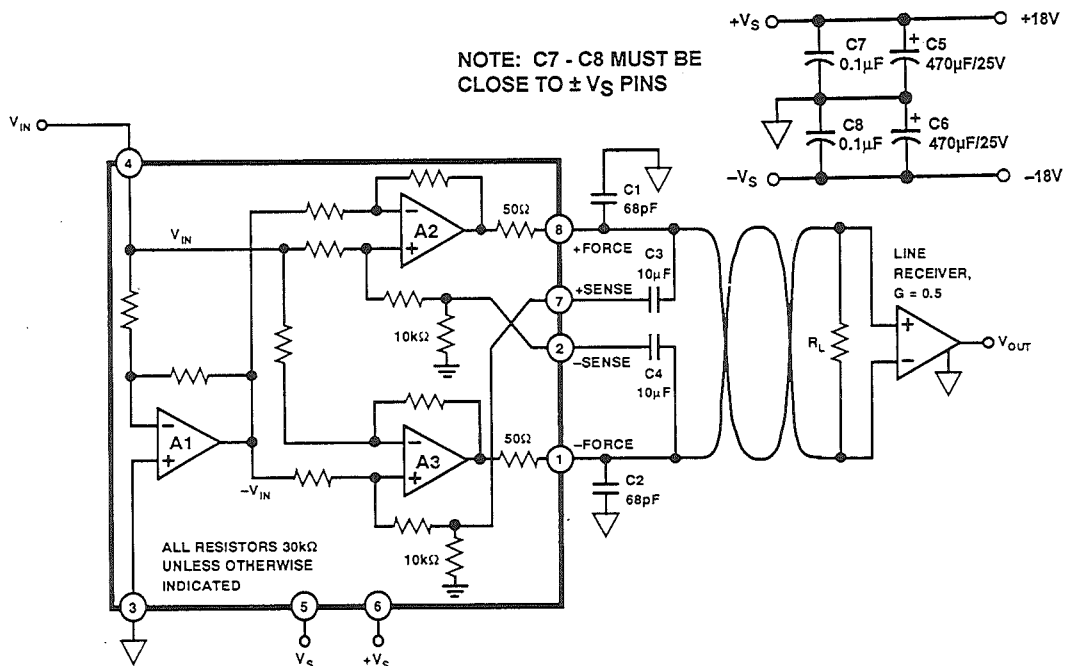


Figure 8.61

The SSM-2142 line driver is designed for a single-ended to differential gain of 2 and will drive a  $600\Omega$  load. In the simplest use, it is simply strapped with the respective output FORCE/SENSE pins tied together (7-8, 1-2). Small film capacitors  $C_1$ - $C_2$  preload the IC for stability against varying cable lengths. To decouple line dc offsets, the optional capacitors  $C_3$ - $C_4$  are used, which should be non-polar types, preferably films. The  $0.1\mu\text{F}$  low inductance bypass caps  $C_7$  &  $C_8$  must be within 0.25" of power supply pins 5 and 6 as long lead lengths will cause excessive THD.

In a system application, the SSM-2142 is used with a gain of 0.5 receiver,

either an SSM-2143, or one of the other line receivers discussed previously. The system shown in Figure 8.61 comprises an entire single-ended to differential and back to single-ended transmission system, with noise isolation, and net unity gain.

Figure 8.62 shows the THD+N performance of the SSM-2142 driver portion of Figure 8.61. Performance is noise limited for the 1V output curve, and distortion drops to  $\leq 0.001\%$  for higher levels, rising with higher frequencies and at 10V output.

## SSM-2142 CROSS-COUPLED DIFFERENTIAL DRIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR $V_{\text{out}} = 1, 2, 5, 10\text{V rms}$ , $R_L = 600\Omega$ , $V_S = \pm 18\text{V}$

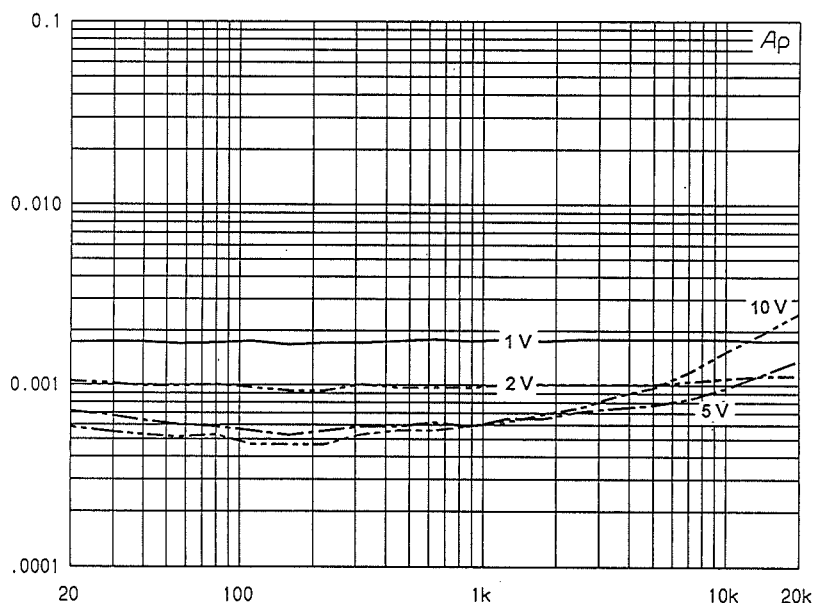


Figure 8.62

## Transformer Coupled Line Driver

Transformers provide a unique method of signal coupling, which allows complete common-mode isolation. As noted in the section on line receivers, transformers are not without their technical and practical limitations, but their singular ability to galvanically isolate grounds maintains a place for them in difficult applications.<sup>[15,16]</sup>

The circuit of Figure 8.63 is a low DC offset, high linearity driver circuit using a high quality nickel core output transformer. U1 and U2 form a high current driver, similar to the current boosted driver of Figure 8.54.

In this circuit U1 is selected as a low bias current, low offset voltage FET

input op amp, in order to hold the DC offset at the primary of T1 to a minimum (less than  $\pm 15\text{mV}$ ). The DC current flowing into the primary winding of a transformer should be minimized, in order to minimize distortion. At the input to U1, C<sub>1</sub> (a high quality film capacitor) decouples any DC offset present on the signal input V<sub>IN</sub>.

The U1-U2 device combination is capable of providing  $\pm 100\text{mA}$  or more, which allows this circuit to drive low impedances. Although T1 is shown with a 1:1 ratio, other winding configurations are possible, allowing the circuit to drive a wide range of load resistances.

8

## TRANSFORMER COUPLED LINE DRIVER

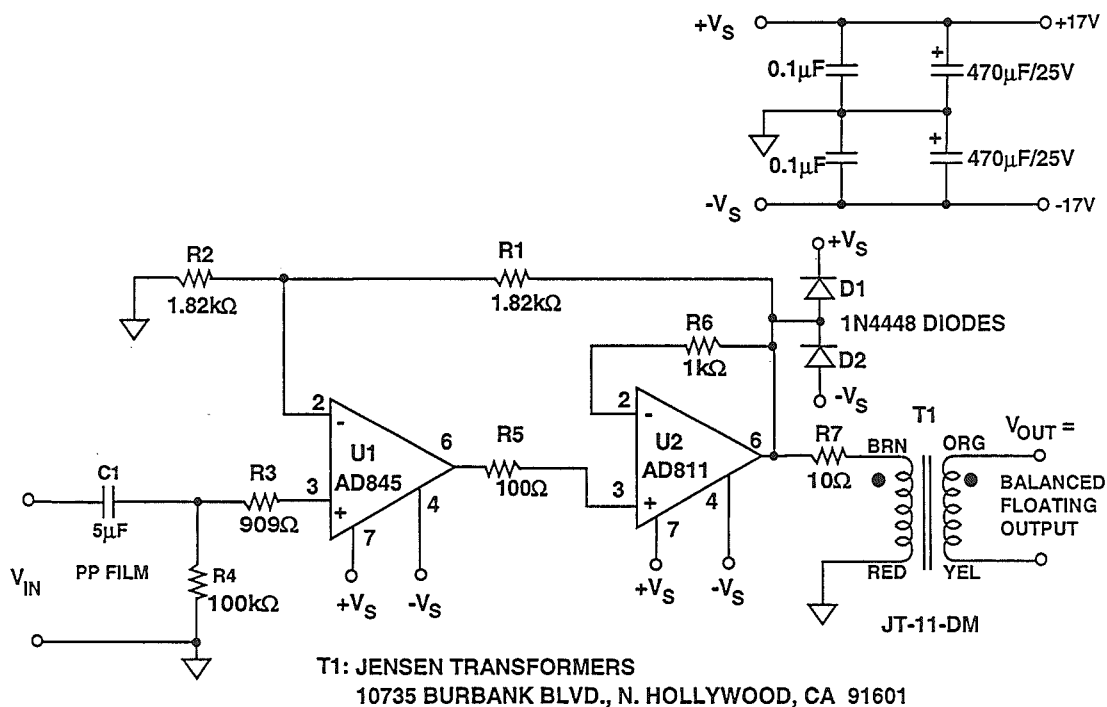
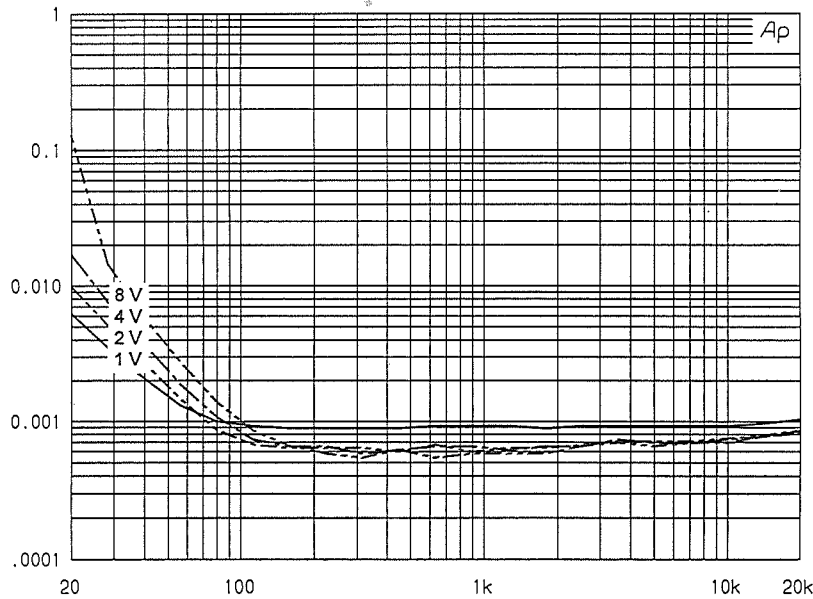


Figure 8.63

**TRANSFORMER COUPLED DRIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 1, 2, 4, 8V$  rms,  $R_L = 600\Omega$ ,  $V_S = \pm 18V$**



**Figure 8.64**

THD+N performance for this driver-transformer combination is shown in Figure 8.64. Like the 2x or 5x basic drivers previously described, its performance is essentially distortion free

above 100Hz. At lower frequencies there is seen a level and frequency dependent distortion rise which reaches a maximum at 20Hz with output levels of 8Vrms (20dBm).

### Transformer Coupled Line Driver with Feedback

Steel core transformers are more economical than nickel core ones, but have higher distortion. To further complicate design, the nonlinear distortion characteristics of steel core transformers vary with level and frequency in a complex way, rising at low levels and low frequencies. Their behavior is less forgiving

than that of the nickel core types, and complicates their use in audio drivers. A family of distortion curves for a typical steel core transformer illustrates this behavior, shown in Figure 8.65. This series of curves is for a Jensen JT-123-S transformer.

# STEEL CORE TRANSFORMER THD + N (%) VERSUS FREQUENCY (Hz) FOR $V_{out} = 5, 2, 1, 0.5V$ rms, $R_L = 600\Omega$

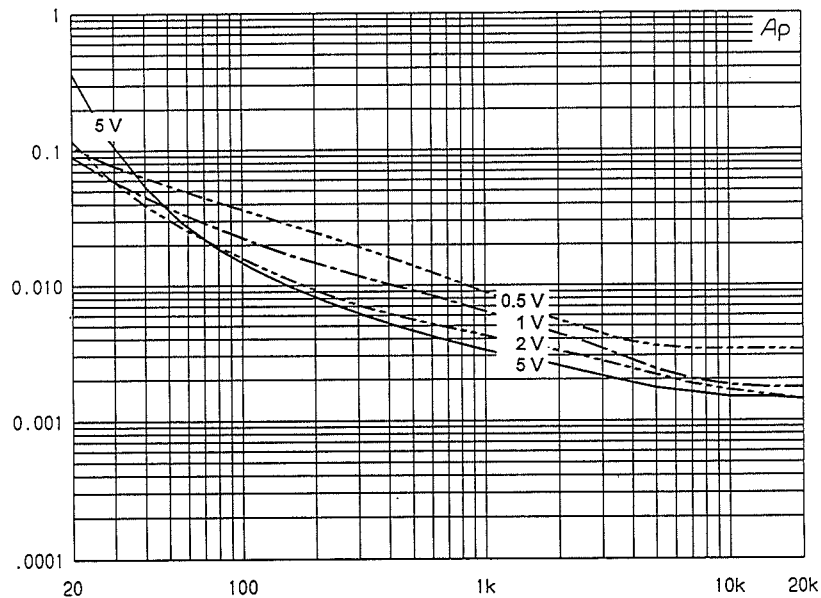


Figure 8.65

## TRANSFORMER COUPLED LINE DRIVER WITH TERTIARY FEEDBACK

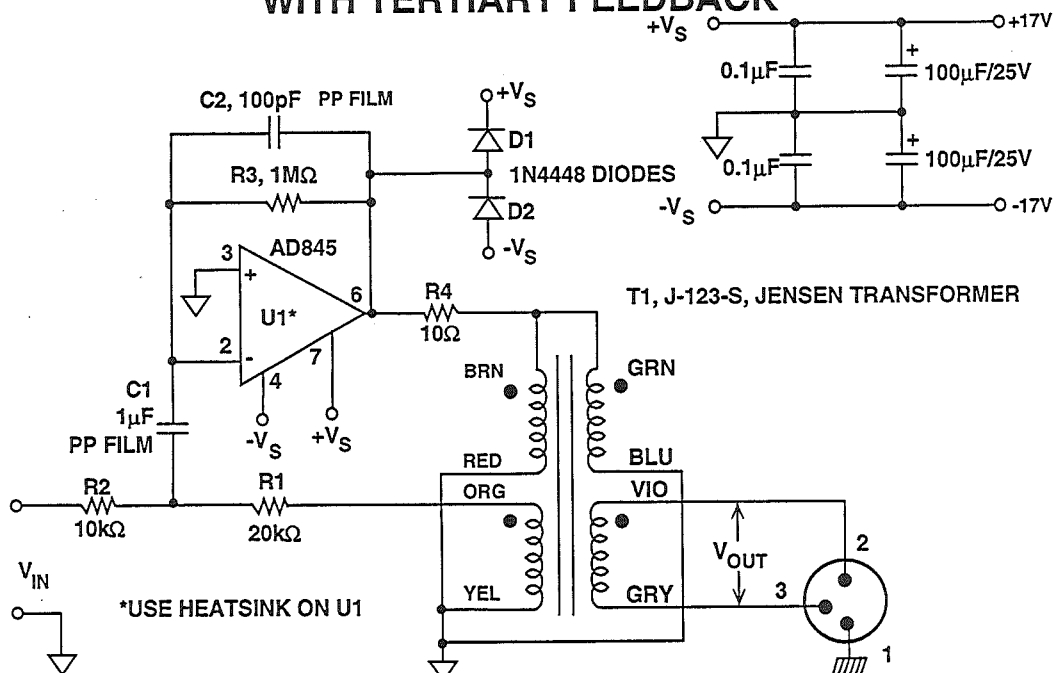


Figure 8.66

If a steel core transformer has several tightly-coupled windings, one may be used in a feedback loop to minimize the effects of the transformer non-linearity.

The circuit of Figure 8.66 is a low distortion driver using the quad-filar wound JT-123-S transformer, and an AD845 as the amplifier. Two parallel windings are used as the primary, feedback is taken from one secondary, and another drives the balanced 600Ω load.

To minimize DC offset, an FET input op amp is used, with local DC feedback via  $R_3$ . This ensures that the maximum DC at the primary is no more than the sum of the amplifier  $V_{os}$  and  $I_{bias} \times R_3$ . For bias currents greater than 1nA and a high value for  $R_3$ , the bias current component may become the dominant DC error. As a consequence a FET input device should be used for U1. Since the AD845 can also dissipate  $\geq 300\text{mW}$ , a heat sink will minimize temperature and hence bias current.

The transformer feedback loop is closed via  $R_1$ ,  $R_2$  and  $C_1$ , which cause the overall U1-T1 combination to act as an inverting amplifier for audio signals. As with a standard inverting amplifier,

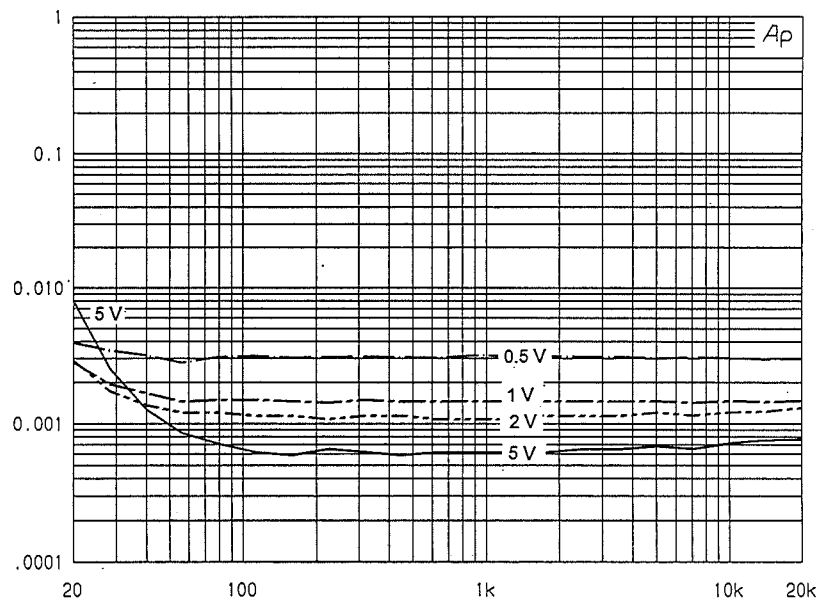
gain is set via  $R_1$  and  $R_2$ , which in this case provide an (unloaded) gain of 2x from  $V_{IN}$  to  $V_{OUT}$ . High quality film capacitors are recommended for  $C_1$  and  $C_2$ , but their exact values and tolerances are not critical.

THD+N performance of this feedback driver is shown in Figure 8.67 using the specified JT-123-S transformer. A comparison of these data with those of Figure 8.65 demonstrates the effectiveness of the distortion reduction, and the variation of distortion with level and frequency. At some points the improvement is more than an order of magnitude.

Some precautions are necessary for the effective use of this circuit; they are mostly concerned with circuit dynamics. The circuit should not be overdriven, particularly at low frequencies, as the resulting distortion can be quite high. Clamping diodes D1 and D2 absorb any inductive kicks from T1 which might damage U1. The output of the basic circuit is limited to just over 5Vrms into 600Ω at low frequencies, but this can be increased by using a buffered driver for U1 (similar to that in Figure 8.63), and a larger transformer for T1.



**STEEL CORE TRANSFORMER WITH FEEDBACK DRIVER**  
**THD + N (%) VERSUS FREQUENCY (Hz)**  
**FOR  $V_{out} = 5, 2, 1, 0.5V$  rms,  $R_L = 600\Omega$ ,  $V_S = \pm 17V$**



**Figure 8.67**

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## APPENDIX: DC SERVO CONTROLLED AUDIO STAGES

With multiple stages of audio-frequency gain, the accumulation of DC offsets in various amplifiers can lead to problems. A classical solution to decoupling DC offset has been to employ input/output coupling capacitors. Typically, this involves the use of large value electrolytic capacitors (100 to 1000  $\mu\text{F}$ ) when operating into low impedances.

Modern low-bias-current, low-offset-voltage op amps allow simple elimination of coupling capacitors in many instances. For example, the use of low bias current, low offset voltage FET

input amplifiers such as AD711/AD712/AD713, AD744/AD746, and OP-249 in a basic gain-of-10 stage will not generally require capacitive coupling. With an appropriate device choice, output offset can be held to as low as  $\pm 10\text{mV}$  or less, and will scarcely vary with source resistance.

This is one approach to the elimination of coupling capacitors. A more general approach which has come into vogue in recent years is the use of a *DC servo amplifier* stage, for output offset elimination.

8

### NON INVERTING GAIN STAGE WITH SERVO

The circuit of Figure 8.68 is a standard non inverting audio voltage-amplifier gain stage (U1), with a non inverting integrator feedback stage connected around it (U2). For normal audio input signals, the gain of this stage is defined conventionally; that is, it is the ratio of the U1 feedback resistance ( $R_2$ ) to the total resistance from the inverting input to ground plus 1. In this instance, the resistance to ground is made up of the parallel equivalent resistances of  $R_3$  and  $R_4$ , so the net gain " $G_{(U1)}$ " of stage U1 is:

$$G_{(U1)} = 1 + \frac{R_2}{R_3 \parallel R_4} \quad \text{Eq. 8.23}$$

In the servo circuit  $R_5$ - $C_1$  and  $R_6$ - $C_2$  form the integration time constants, which should be well matched in this form of integrator. The DC feedback from stage U2 is applied to the inverting input of U1 via  $R_4$ . The servo loop forces the net DC output of amplifier stage U1 to a very low level. In practice, the DC output offset of U1 becomes equal to the offset voltage of amplifier U2.

Two factors affect the low frequency rolloff of the U1 gain stage, as altered by the servo loop. One is the integrator RC time constant, which sets the integrator stage's -3dB frequency point,  $f_{(U2)}$  (not the overall system -3dB point). The integrator 3dB point is:

## NON-INVERTING GAIN STAGE WITH DC SERVO

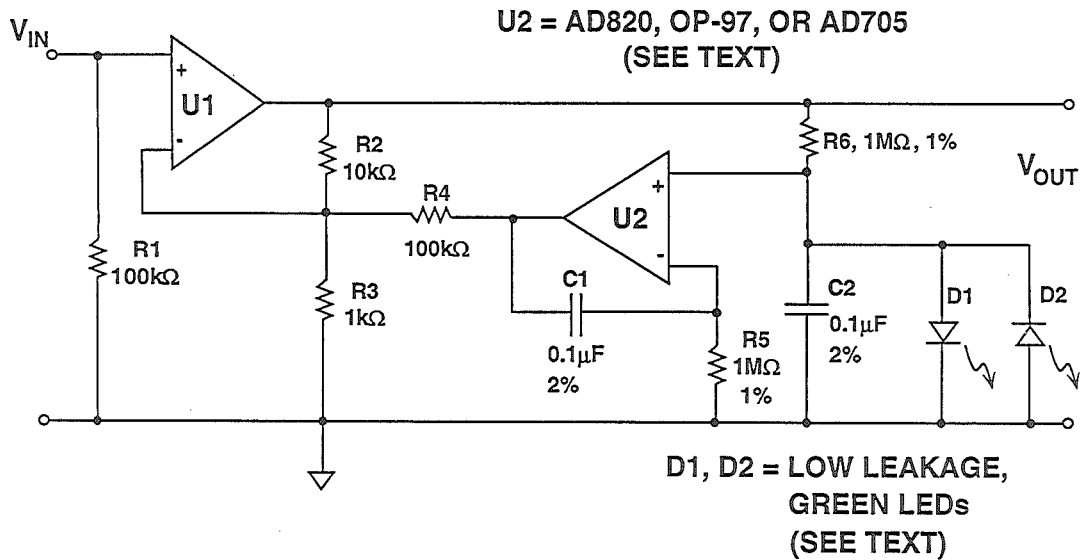


Figure 8.68

$$f_{(U2)} = \frac{1}{2\pi R_5 C_1} \quad \text{Eq. 8.24}$$

where  $R_5 = R_6$ , &  $C_1 = C_2$ .

A second factor is the total DC transfer ratio of the circuit, measured from the U2 input to the U1 output, or servo sense point. If this is defined “1/n”, then a modified expression for the overall circuit’s -3dB point can be written as:

$$f_{(3dB)} = \frac{1}{n 2\pi R_5 C_1} \quad \text{Eq. 8.25}$$

where  $n = R_4/R_2$ , thus:

$$\frac{1}{n} = \frac{R_2}{R_4} \quad \text{Eq. 8.26}$$

The servo RC values should be selected first for reasonable values. Then, feedback resistor  $R_4$  is chosen several times higher than  $R_2$ , making “n” large and “1/n” small. In the example, 1/n is 0.1,

so the the rolloff point is about 0.16 Hz. In general the rolloff frequency should be around 1% of the low frequency limit of the signal being processed.

At the U2 amplifier input, low-leakage ( $\leq 100$  pA) clamp diodes should clamp  $C_2$ , to prevent possible latch up. Suitable diodes are ordinary green LEDs with a light shield such as shrink tubing (to eliminate photocurrents), or C-B junctions of 2N5088/89 NPN transistors. Servo amplifier U2 should be a unity gain compensated, low offset voltage, low-input-bias-current op amp. This can be either a FET-input device or a bias current compensated super- $\beta$  bipolar. Possible choices are the AD711 or the OP-41 (FETs); or an OP-97 or AD705 (bipolar).

Note that most FET input op amps will need the clamp diodes to prevent phase reversal. When working on a common rail design (i.e., both the servo amplifier and amplifier being servo'd operate from common rails), there are exceptions to this behavior. These are the AD820 and AD822 op amps, which, as single supply designs, have working input CM ranges which include the negative rail. As such they can be used without special precautions against latchup, and they also serve very well as integrators due to their very low bias current of 2pA and their rail-rail output swing. Given these characteristics, the AD820 and AD822 are especially suitable for the application.

Any servo amplifier IC working on supplies lower than that of the servo'd

amplifier must use the clamping diodes. An audio power amp, for example, may swing  $\pm 50$ V at its output, and such potentials can cause malfunction or outright destruction in lower voltage servo ICs.

U1, and its associated circuitry, can take on many forms more complex than the one in this basic example. U1 might be a high output swing power amplifier. The servo loop would still operate as described, and correct not only offset errors due to U1, *but also any varying DC input level to U1*. The servo technique can be useful for continuous correction of high bias current, high offset or high drift. (It will even stabilize thermionic valves—another exercise for the historically minded reader).

Ensure that the worst-case offset to be corrected at the input of U1 is within the dynamic range defined by the values assigned for  $R_2$ - $R_3$ - $R_4$ , the specific supply voltages used for U1-U2, and the clamps. High-quality low-leakage 1 or 2% film capacitors should be used in the integrator along with 1%, 50ppm/ $^{\circ}$ C metal-film resistors. Since these components will be high-impedance, lead lengths should be minimized around U2, and the assembled circuit should be carefully cleaned of any flux residue. The outside foils of both  $C_1$  and  $C_2$  should be connected to the lower impedance of the two nodes.

## INVERTING GAIN STAGE WITH SERVO

An inverting stage with servo offset correction is shown in Figure 8.69, and uses a familiar inverting integrator for feedback. In this circuit, U1 is an in-

verting audio stage with a gain of  $R_2/R_1$ . DC feedback from the U2 integrator stage is applied to U1 through the divider,  $R_4$ - $R_3$ .

### INVERTING GAIN STAGE WITH DC SERVO

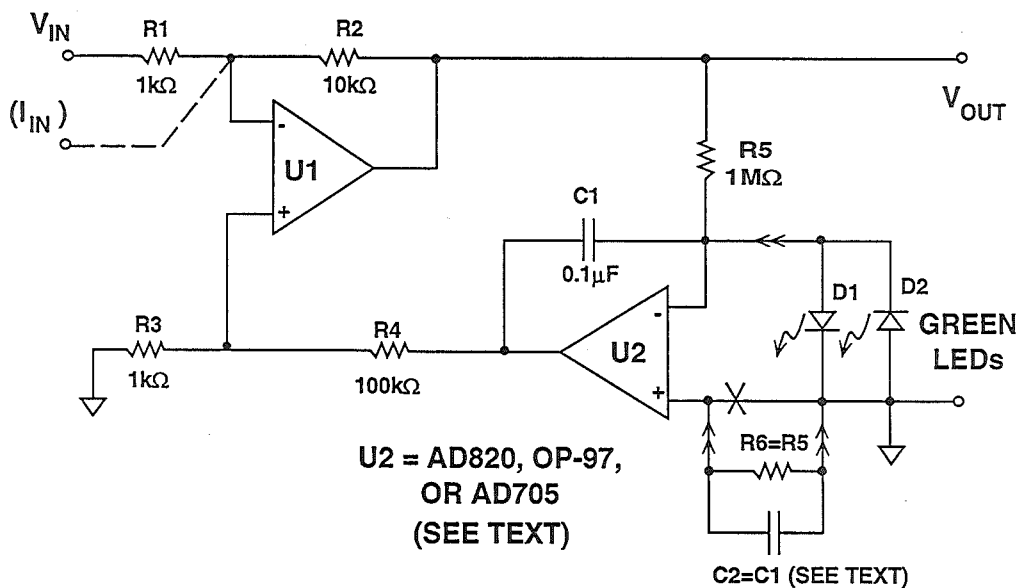


Figure 8.69

In this circuit the  $1/n$  scaling factor around the U2-U1 DC loop is:

$$\frac{1}{n} = \left( \frac{R_3}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) \quad \text{Eq. 8.27}$$

which is used to calculate the circuit's effective rolloff. With the time-constant values shown and the scaling of  $R_4$ - $R_3$ , the circuit of Figure 8.69 has a low frequency cutoff of about 0.17 Hz.

When used just as shown with the U2 noninverting input grounded, clamping

diodes may not be necessary if they are integral to U2, as they are in the AD705 and OP-97. For higher bias current amplifiers at U2, the compensation network  $R_6$ - $C_2$  may be used, in which case low-leakage input clamp diodes are recommended. In any case, the use of quality components for  $R_5$

and  $C_1$  is important. Again,  $R_4$  should be about ten times  $R_2$  (with  $R_1$  and  $R_3$  equal), and the supply voltage used for U1-U2 must be sufficient to accommodate the worst DC offset expected of U1. This circuit also works with more complex inverting stages, including discrete ones.

In principle, a *non inverting* integrator could also be used, with DC feedback to the  $R_1$ - $R_2$  junction. The inverting integrator is more simple overall, however, and eliminates one RC network. This circuit works well when U1 has a current input.

From a system point of view, the "1/n" scaling factor of the servo can be very useful in extending the low frequency range of these two basic designs. A DC

attenuator or "tee" network can be placed between the U1 output and the integrator, and will work in a similar fashion for 1/n frequency scaling.

However, this particular frequency scaling approach should be used with caution, as it has the side effect of increasing the input offset of integrator U2 by the amount of attenuation. The output offset of U1 is then higher. For modest attenuations prior to the integrator ( $\leq 10$  times), the circuit can be useful with the AD705 or OP-97 or similar devices, as their worst case offset is below  $100\mu\text{V}$ . In general, the offset multiplication effect prevents most amplifiers from being used with substantial ( $\geq 10$  times) input attenuation prior to  $R_5$ .

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#### **Acknowledgments:**

In the preparation of this material the author was aided by helpful comments and other inputs from a number of parties. Thanks for these go to Gary Galo of the Crane School of Music, to Ben Duncan of Ben Duncan Research, to John Curl of JC Designs, to Steve Hogan and Bill Whitlock of Jensen Transformers, to Jay McKnight of Magnetic Reference Laboratory, to Jill Sprague of MicroSim, and to Neil Muncy of Neil Muncy Associates. Thanks go also to those ADI associates who commented on various portions of the manuscript.

Portions of this material were adapted from the author's **Audio IC Op Amp Applications**, 3d Ed., Howard W. Sams, 1987.

## SPEAKER CROSSOVERS

### *Hank Zumbahlen*

The physics of sound reproduction make it very difficult for one driver (loud-speaker) to handle all audio frequencies. Therefore, most speaker systems consist of multiple drivers, each reproducing a segment of the audio spectrum. A mass-controlled piston working into an acoustic load derives its response curve from the cancellation of

two opposing effects. First is the cone excursion which is inversely proportional to the square of the frequency. The second is the resistance of the acoustic load which is proportional to the square of the frequency. These effects cancel in the center of a speaker's frequency response, creating a flat response.

## SPEAKER CROSSOVER CONSIDERATIONS

- Frequency Division Between Speakers
- Speaker Impedance Versus Frequency (Compensation)
- Component Selection
- Passive Versus Active Crossover Networks

Figure 8.70

At some high frequency, where the wavelength of the acoustic wave is less than the circumference of the driver; the acoustic resistance levels off, and the response of the speaker rolls off at 12 dB/octave. At the resonant frequency of the driver, the excursion is dominated by the compliance of the suspension rather than the mass of the cone.

This causes a roll off which is also 12 dB/octave. Therefore, reproduction of low frequencies requires a speaker that has a large surface area, allowing it to move a large amount of air. The driver surface should also have relatively high stiffness so that the surface moves as a uniform piston with no flexing. This usually implies higher mass.

For high frequencies, the tweeter should have as little mass as possible so that it can respond to the input signal quickly. Even though a zero-mass tweeter would be ideal, the tweeter still needs stiffness so that it does not flex.

Most speakers work well over a frequency range of about 10:1. This means that we would customarily use three drivers to cover the audio spectrum of 20 Hz to 20 kHz. For reasons of simplicity (and cost), designers sometimes try to cover the frequency spectrum with only two drivers. This places higher demands on each driver and usually requires sharper cutoff rates on the crossover filter to limit the out-of-band driver signals. It is especially important to limit the low frequency energy to the tweeter in order to limit its excursion.

Since we have separate speakers covering different portions of the spectrum, we need to divide the input signal spectrum and then direct the proper portions to the proper drivers. These crossovers are usually passive filters placed between the power amplifier and the drivers. Sometimes, however, we may want to implement the crossover function at line level. There are some advantages as well as disadvantages to this approach.

The passive crossover is simply a high-level passive filter. The speaker is the

load impedance of the network. We generally assume zero source impedance (as opposed to using a source termination). This ensures the maximum power is delivered to the load. Next we determine the crossover type. The two configurations used most often in speaker crossover design are the all-pass configuration (APC) and the constant-power configuration (CPC).

The APC, introduced by Garde, is the current favorite. When the outputs of the filters are combined, the resultant has the same magnitude as the input at all frequencies. This is shown in the following equation (Eq. 1) where  $V_{IN}$  is the input voltage,  $V_L$  is the low pass output voltage,  $V_M$  is the bandpass output voltage and  $V_H$  is the high pass output voltage. Phase does not appear in this equation.

$$|V_L + V_M + V_H| = |V_{IN}| \quad \text{Eq. 1}$$

It is not possible to pass a signal through a ladder network and preserve both magnitude and phase. APCs are desirable because they do not introduce variations in the speakers amplitude response.

The other popular network is the CPC (constant power crossover). In the CPC, the output *power* of the network is equal to the input (Eq. 2).

$$|V_L|^2 + |V_M|^2 + |V_H|^2 = |V_{IN}|^2 \quad \text{Eq. 2}$$

The use of this type of crossover predates the APC in commercial systems by many years. It is interesting to note that odd-order systems are both APC and CPC.

The next thing that must be determined is the order (number of poles) of

the system. All-pole systems roll off at 6n dB/octave, where n is the order.

First order systems are attractive because few components are required. However, because of the low rolloff rate, the response of the drivers must be flat far beyond the crossover frequency. As

a practical matter, the speaker responses overlap so much that problems such as interdriver cancellation are more troublesome. (Interdriver cancellation occurs when two drivers operate at the same frequency, and the speakers are separated by an odd multiple of  $1/2$  the wavelength of the signal.) A first order system is a minimum phase system as well.

Second order systems are considered by many to be the lowest acceptable order for a crossover network. The number of components is still manageable, the operational range is better controlled, and the phase shift of the network is still quite low. In contrast to odd order

crossovers, 2nd order (and all even order) crossovers are insensitive to system phase relationships.

Third order systems are also very popular. Since they are odd order, they are both APC and CPC. The number of components is still manageable, but the phase shift of the network is greater.

Fourth order systems are sometimes used where a high cutoff rate is required (often to reduce the excursion of a tweeter). The disadvantages of fourth order systems are high component count (high cost), and high phase shift in the network.

## IMPEDANCE COMPENSATION

All design equations for crossover networks assume a constant load impedance. The impedance of a speaker is far from constant as shown in Figure 8.71. We should therefore add networks

to try to equalize this impedance. Typically, this network takes the form of a series R-C across the speaker terminals (called a Zobel network) as shown in Figure 8.72.

## SPEAKER IMPEDANCE

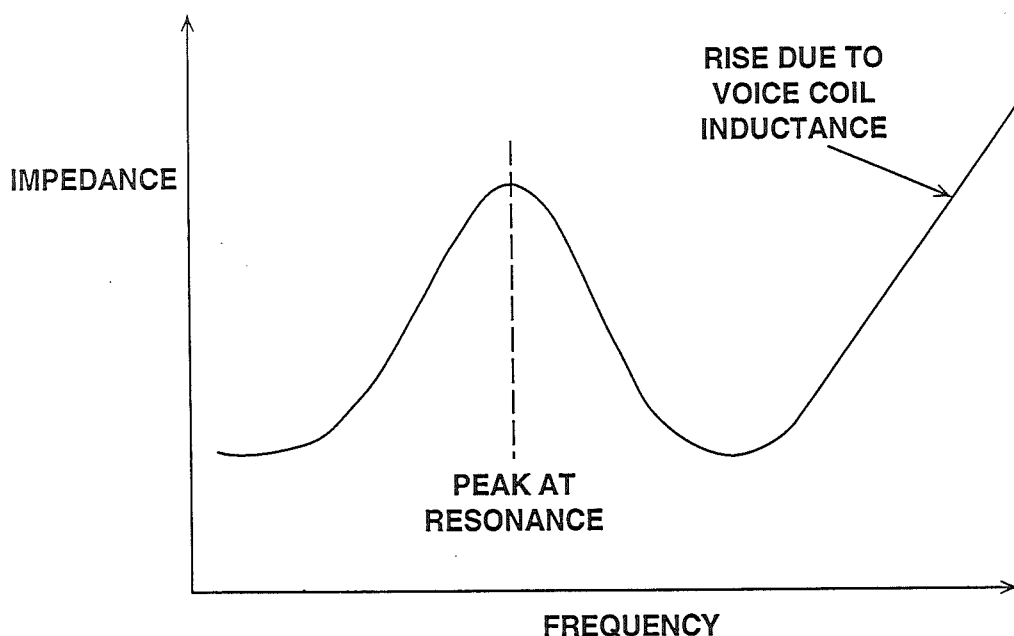


Figure 8.71

## ZOBEL NETWORK

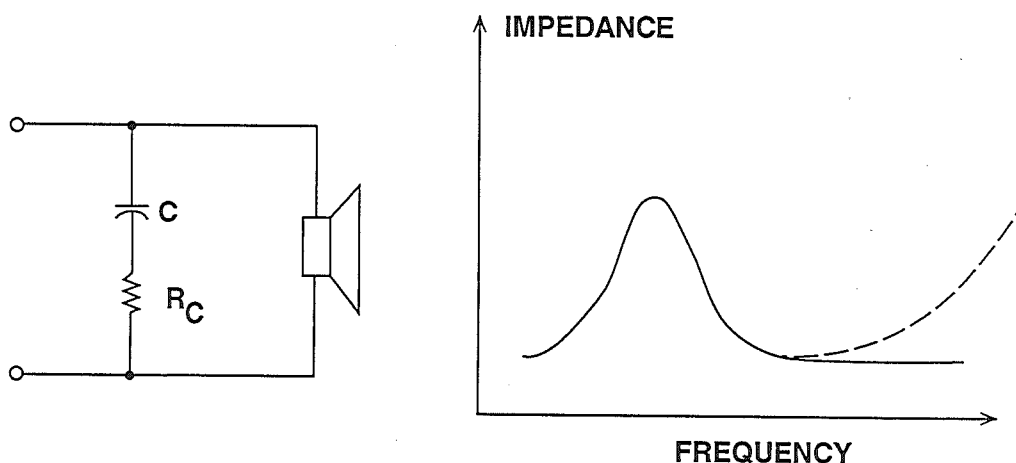


Figure 8.72

Unfortunately the Zobel network only partially compensates for the speaker impedance variation. The impedance of the speaker does not rise with frequency as a series L-R network does, but is approximately proportional to  $R\sqrt{L}$ . This is sometimes referred to as a *semi-inductor*. However, the simple Zobel network, optimized at the crossover frequency, does a good job of flattening the impedance in the frequency range around the crossover where it is needed most (see Figure 8.72).

There is an impedance peak at the resonant frequency of the speaker. This peak has a fairly high  $Q$ . We can design a series LRC network to equalize this peak as shown in Figure 8.73. However,

as the frequency goes down, the size of the inductor required (in value, physical size and cost) becomes large. Compensation of this type is therefore rarely used for woofers, but is more common for midrange drivers and tweeters, especially when the resonant frequency is within an octave of the crossover frequency. Since these are high  $Q$  circuits, the transient response is not optimum and they tend to ring.

You can also add networks in series with the speakers to control frequency response variations. These networks are usually parallel LR (for rising response with frequency, Figure 8.74A), RC (for falling response with frequency, Figure 8.74B), or LRC (for a hump in the frequency response, Figure 8.74C).

## RESONANCE COMPENSATION

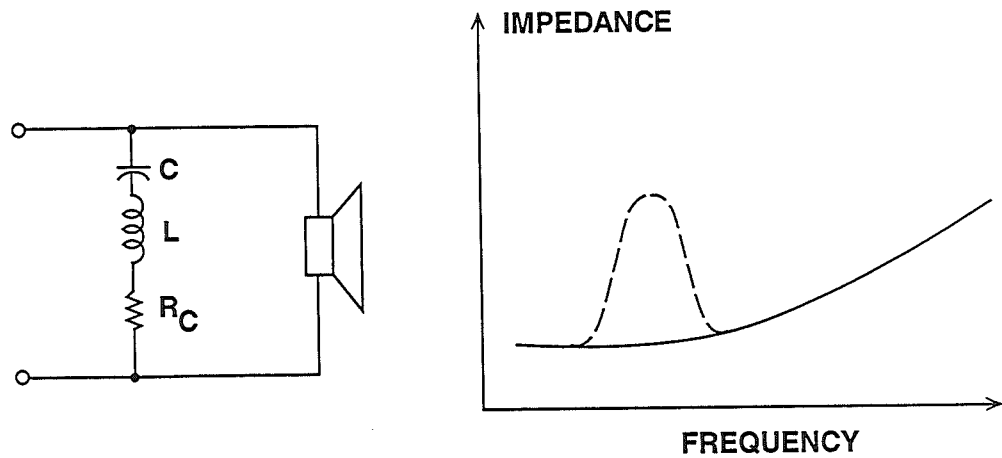


Figure 8.73

## SERIES NETWORKS OFTEN USED TO CONTROL SPEAKER IMPEDANCE

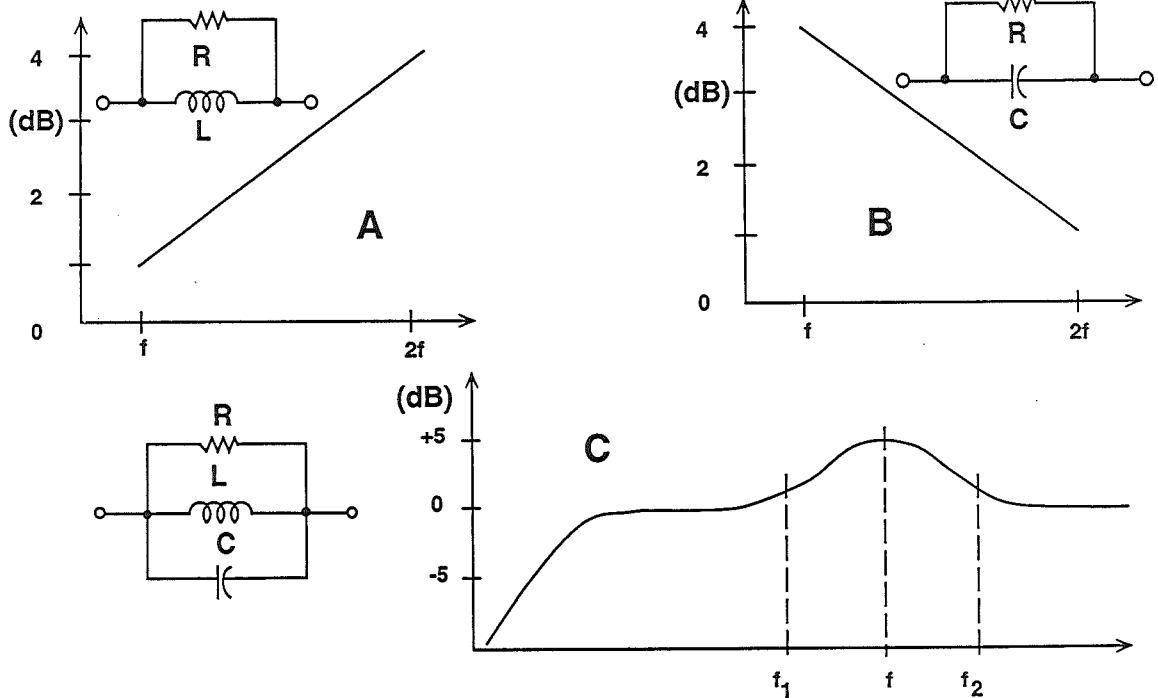


Figure 8.74

A last function which should be accomplished by the crossover is to equalize the sensitivities of the drivers. This is normally accomplished with an L-pad so that the signal level can be adjusted without affecting the load impedance seen by the network. An alternative is to use a resistor in series with the load. The crossover load is now the sum of the pad resistor and the speaker impedance, which still requires impedance equalization. This approach, while saving a resistor, does not allow the flexibility of adjustment offered by the L-pad.

The quality of the components used is crucial to good performance. *Inductors* should have low DC resistance because of the high currents they will carry. These currents may actually be larger than the ones in the load. The currents can approach tens of amperes. Since the impedance levels are low, it only takes a small amount of resistance to turn a LC network into a LRC network. The formulas for passive crossovers assume ideal inductors with no series resistance. This means that the inductor must be wound with thick wire. Most crossover inductors are wound with AWG 16 or 14 wire. Iron core inductors should be designed so that they do not saturate under high peak current

conditions. Many audiophiles dislike iron core inductors for this reason, but they do allow higher inductance values for a given amount of wire and provide lower DC resistance.

*Capacitors* for audio use should have a film dielectric. Electrolytic capacitors should be avoided. Their ESR (equivalent series resistance) and DA (dielectric absorption) are poor and, being polarized, their behavior with an unpolarized audio signal (the commonest sort) is distinctly non-linear. Unfortunately, film capacitors are only available up to about 100 $\mu$ F, and at these values, they are very large.

*Resistors* should be large enough to absorb at least as much power as that being delivered to the speaker. Square power resistors are the best choice. They are inexpensive, fairly accurate, and they are resistive rather than reactive throughout the audio frequency range.

The physical size of the components, the series resistance of even high quality inductors, and the limitations imposed by the speaker as the terminating load compromise the accuracy of the passive crossover. This has led designers to consider active crossovers as an attractive alternative.

## CROSSOVER DESIGN EXAMPLE

Our goal is to design a three-way (woofer, midrange & tweeter) system. The midrange driver is actually three drivers in parallel, and the tweeter is two drivers in parallel. The drivers' voice coils are arranged in parallel instead of in series for two reasons. First, a solid-state amplifier is more

likely to develop large currents at moderate voltages than large voltages at moderate currents. So it is better to have a low impedance system. Secondly, the power at resonance divides more uniformly between drivers in parallel than between drivers in series. Physically, the midranges and tweeters



alternate in a line-array arrangement. This is variation on the D'Appolito configuration. This configuration has the advantage of a very uniform horizontal frequency response.

First we measure the impedance of the speakers versus frequency. We use the setup of Figure 8.75. This approximates

a constant current source. We first substitute a  $10\Omega$  resistor for the speaker. We then adjust the level of the oscillator for  $10\text{mV}$  across the resistor. Now, leaving the oscillator level fixed, we replace the speaker and measure the impedance directly;  $1\text{mV}$  corresponds to  $1\Omega$  impedance.

## IMPEDANCE MEASURING

8

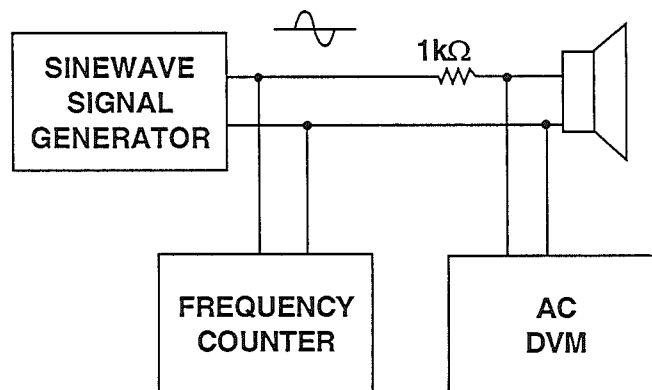
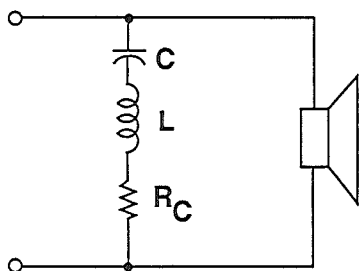


Figure 8.75

As it is desirable to load the passive filter with a fixed impedance, the impedance versus frequency should be as flat as possible.

The design equations shown in Figure 8.76 and Figure 8.77 are now used to determine the passive crossover network component values (Figure 8.78).

## RESONANCE COMPENSATION NETWORK DESIGN



Design Equations:

$$C = \frac{0.1592}{R_E Q_{ES} f_s}$$

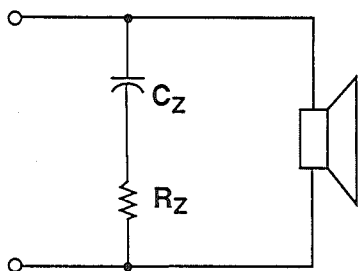
$$L = \frac{0.1592 R_E Q_{ES}}{f_s}$$

$$R_C = R_E + \frac{Q_{ES} R_E}{Q_{MS}}$$

Obtain From Speaker Manufacturer's Data Sheet:  $Q_{ES}$ ,  $Q_{MS}$ ,  $R_E$ ,  $f_s$

Figure 8.76

## ZOBEL COMPENSATION NETWORK DESIGN



Design Equations:

$$R_Z = 1.25 R_E$$

$$C_Z = \frac{L_E}{R_Z^2}$$

$L_E$  = Driver Voice Coil Inductance in Henries

Figure 8.77

## IMPEDANCE MATCHING NETWORKS

DRIVER	C	L	R <sub>C</sub>	C <sub>Z</sub>	R <sub>Z</sub>
Midrange	466 $\mu$ F	1.23mH	2.4 $\Omega$	23.2 $\mu$ F	2.2 $\Omega$
Woofer	7538 $\mu$ F	9.3mH	3.0 $\Omega$	66.9 $\mu$ F	3.5 $\Omega$

NOTE: TWEETER REQUIRES NO IMPEDANCE COMPENSATION

8

Figure 8.78

The capacitance value of 7538 $\mu$ F for impedance compensation (C, L & R<sub>C</sub>) is not practical for the woofer because the frequency of the impedance peak is so low. We will therefore ignore this part of the compensation. If this were a ported enclosure, the impedance hump would actually be partially tuned out by the enclosure. This would reduce the large hump and add an additional smaller hump. This system is a transmission line, however, which tends to flatten impedance peaks.

For the remaining components we use the nearest standard value for the inductors and resistors. We synthesize the desired capacitor values by paralleling standard values. The 466 $\mu$ F capacitor is made by paralleling 280 $\mu$ F +

140 $\mu$ F + 47 $\mu$ F. Because of the size of the capacitors, we are forced to use electrolytics for values >100  $\mu$ F. This is not a significant problem in this design, since the resonant tank circuit functions over a relatively small frequency range. Also, since it is a shunt circuit, its effects are not heard in the speaker. In addition, the frequency of the resonance is low so the ESR of the cap is minimized. To eliminate the requirement of a polarization voltage, we use non-polarized electrolytics (back-to-back electrolytics arranged so that either one or the other is properly polarized). The effectiveness of this compensation is shown in Figure 8.79 for the woofer and in Figures 8.80 and 8.81 for the midrange driver.

## WOOFER IMPEDANCE

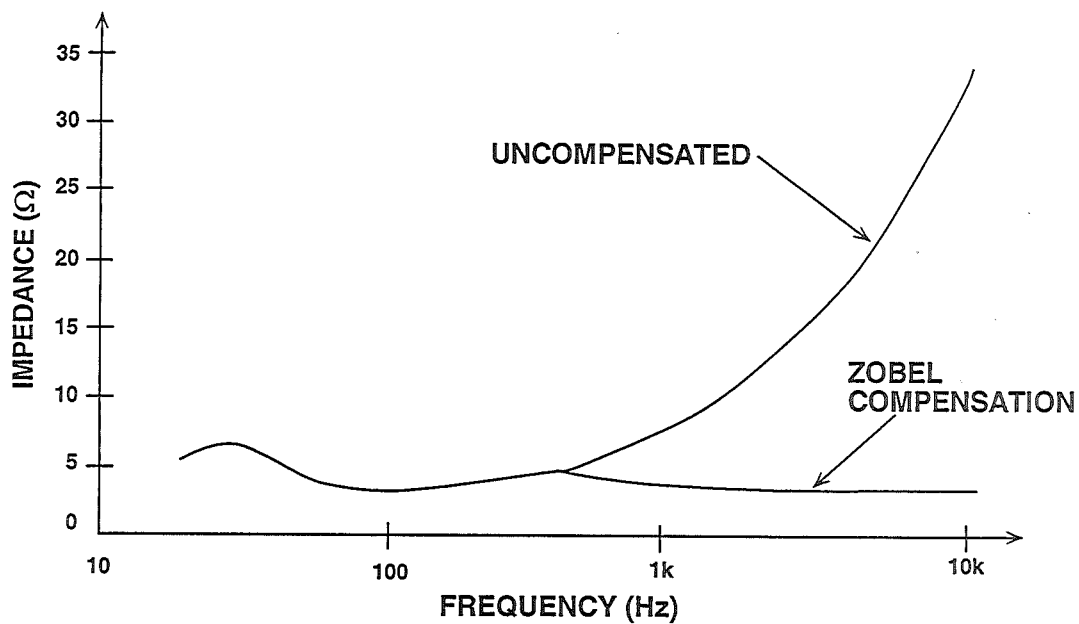


Figure 8.79

## MIDRANGE IMPEDANCE

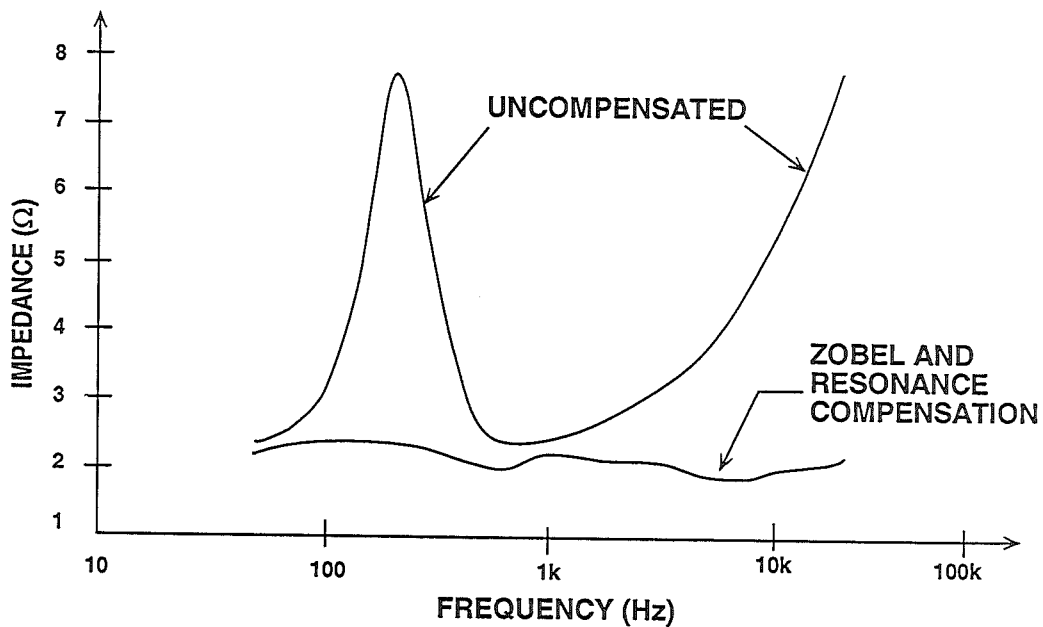


Figure 8.80

## MIDRANGE IMPEDANCE

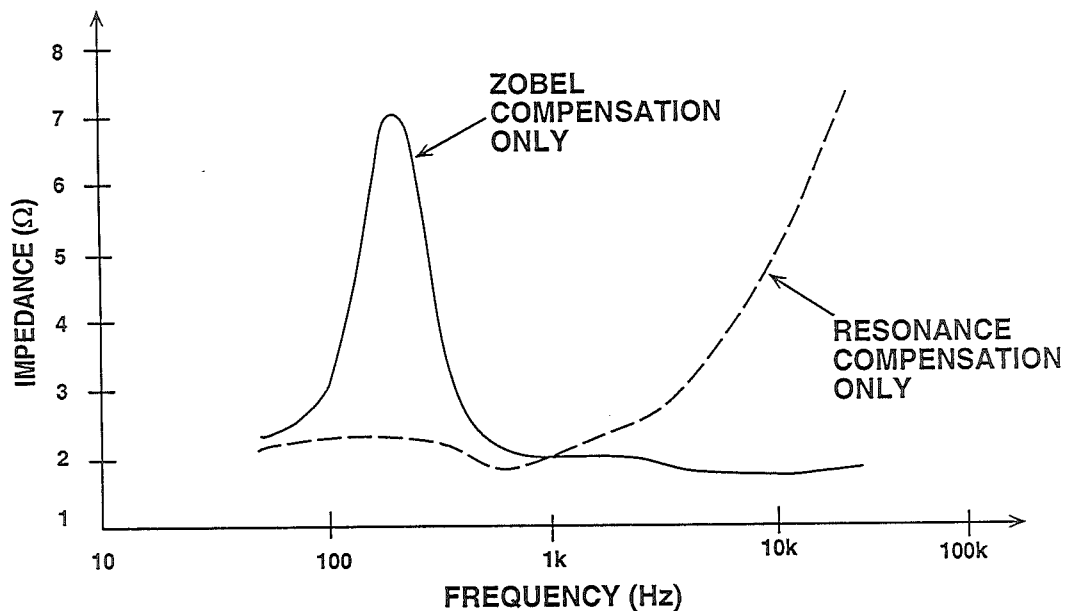


Figure 8.81

We do not attempt to compensate the tweeter because the impedance peak is relatively small and far away from the tweeter passband. Also, the impedance does not begin to rise with frequency until beyond 20 kHz. While this is true of this particular set of drivers, it is not necessarily so, and impedance compensation may be required if other drivers are used.

With the speaker impedances compensated, we design the actual crossovers. We choose a 2nd order APC. We start by using the equations of Bullock in his

classic series on crossovers in *Speaker Builder* (1/85 - 3/85, 1/86 & 4/87). The equations were put into a spreadsheet to allow for easy manipulation of the numbers. The cutoff frequencies were then modified slightly so that the inductors required fall as close as possible to standard values. The calculations used are in Appendix 1. The capacitor values are synthesized by paralleling standard values. The final schematics are shown in Figures 8.82, 8.83, and 8.84. Note that the polarity of the midrange drivers are reversed. This is critical for the proper response.

## WOOFER COMPENSATION CIRCUIT

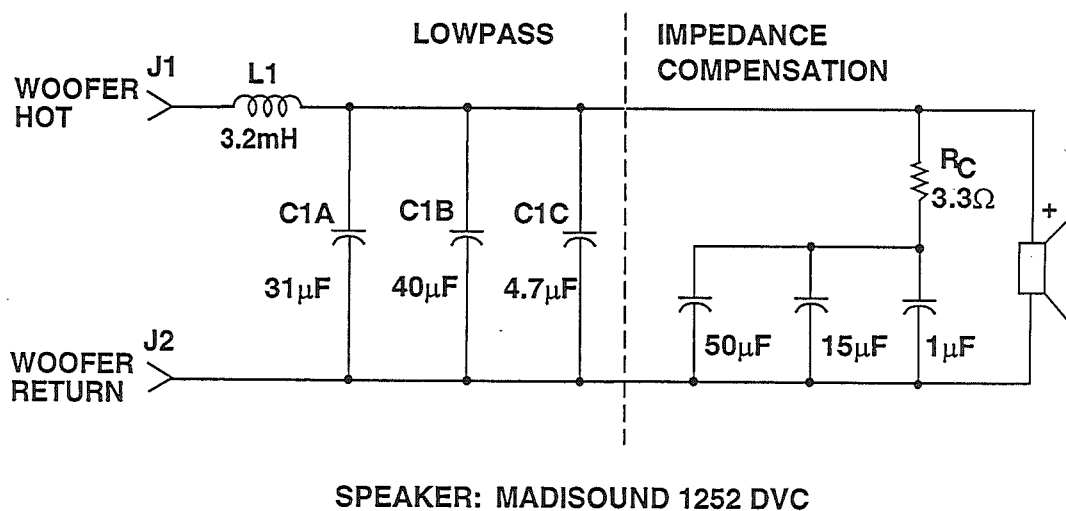


Figure 8.82

## MIDRANGE COMPENSATION CIRCUIT

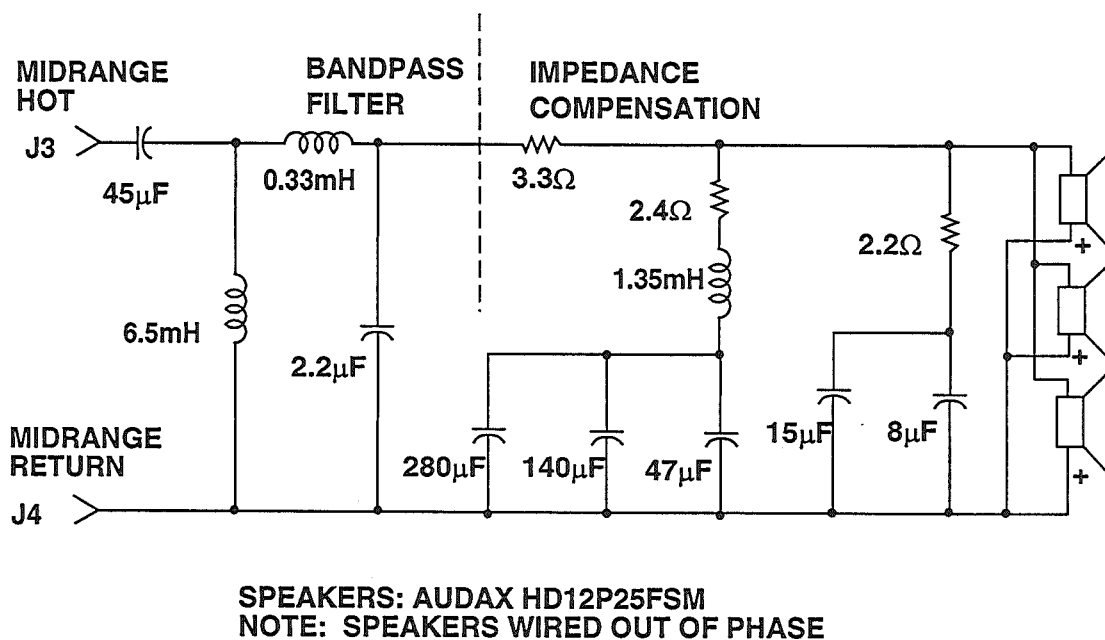


Figure 8.83

## TWEETER COMPENSATION CIRCUIT

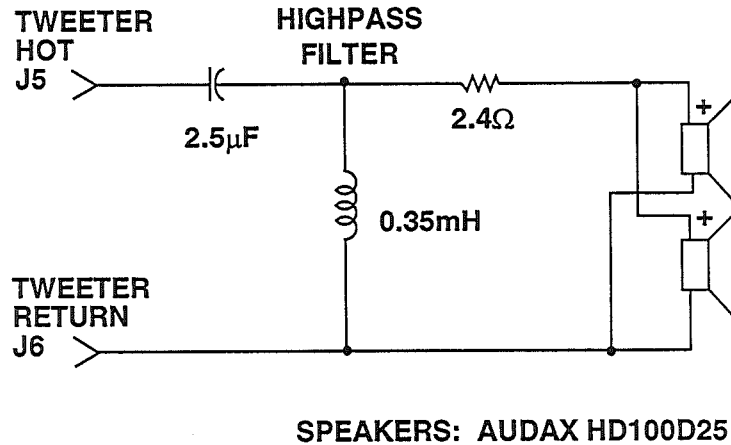


Figure 8.84

Some final points regarding the passive crossover are in order. If the inductors are oriented so that their magnetic fields overlap, unwanted voltages may be induced from one inductor to the other by mutual inductance. This can be avoided by orienting coils in close proximity and at right angles to each other.

In wiring the drivers, use two separate wires (hot and common) to each set of

drivers rather than use a common return for all drivers. This minimizes inductance and impedance in the return path and prevents the modulation of one speaker by the other. This idea may be extended by providing two separate cables between the power amplifier and the speakers: one for the woofer, and one for the midrange and tweeter. This is referred to as *bi-wiring*.

### Active Crossover Network Design

Active crossovers are active filters which partition the frequency spectrum. They are line level circuits which are placed in front of the power amplifiers. A separate power amplifier is therefore required for each frequency range

speaker. This is the active crossover's chief disadvantage. Since a separate amplifier is required for each band, the cost of the system is much higher. However, there are many advantages to active crossovers.

## PASSIVE VERSUS ACTIVE CROSSOVERS

PASSIVE	ACTIVE
■ Large, Expensive Components	■ More Component Spread Allowed
■ Difficult to Design and Manufacture	■ Easier to Tune
■ Simple Interface	■ Better Amplifier Control of Driver
	■ Increased Power Amp Requirements
	■ More Costly than Passive
	■ Time Domain Compensation Possible

Figure 8.85

First, the active crossover network is isolated from the speaker impedance by the power amplifier. This makes the design of the filter simpler and more accurate. Second, the impedance of the filter may now be scaled so that component values can be made more practical. Another advantage is that inductors are not used in active filters, and it is much easier to tune an active filter than a passive filter because of the isolation between the sections of the active filter.

Another possible feature which can be implemented in an active crossover is time delay. The acoustic center of a speaker is located approximately at the point where the voice coil attaches to the cone (or dome). When different speakers are mounted on a common baffle, their acoustic centers do not line up. This results in a time difference

which can be canceled by delaying the signal to one speaker relative to another. This can be accomplished with an all-pass filter. Time alignment can also be accomplished by mounting the different speakers on baffles that are offset from each other. However, this increases manufacturing difficulty and may cause problems with diffraction around the baffle edges.

In the active design, impedance matching circuits may be eliminated. Almost all modern audio power amplifiers have very low output impedances at audio frequencies. This means that they will provide whatever current is required (within the amplifiers' current output capability), to develop the correct voltage across the load. Therefore, speaker impedance changes with frequency do not affect overall performance.



Another advantage of an active crossover is that since the speakers are connected directly to the amplifier, the damping ratio of the amplifier can control the back-EMF of the speaker. This is especially true for the woofer. A dynamic driver works by developing a voltage in a coil of wire (in this case called a voice coil) which then moves relative to a fixed magnet. Back-EMF is produced by the speaker's voice coil moving through a magnetic field due to the momentum of the cone, not because of an input signal. This sets up a voltage in the coil. If the coil is connected to a low impedance source, such as the power amplifier, the induced voltage is essentially shorted out. If there were a passive crossover between the speaker and the driver, this back EMF would distort the signal because of the finite driving impedance. Eliminating this effect results in better transient behavior (i.e., "faster" bass).

We can now design the active frequency crossover network. We would typically use a standard filter realization such as the Sallen and Key or Multiple Feedback (MFB). For a second order filter, the "a" parameter in Bullock's article is  $\alpha$  (1/Q) for the filter. The "H" parameter is the gain peaking function of the bandpass. If we had used a CPC filter we would probably implement the active crossover as a Butterworth filter of the proper order. For an APC filter it is more complicated if the proper response is to be maintained, as the equations are a function of the spread in the two crossover frequencies.

First select the circuit topology. It may seem attractive to form the bandpass section by subtracting the lowpass and highpass sections from the input signal. The problem with this approach is that the response does not turn out the way that we would expect.

Take for example subtraction of a lowpass from the input signal to form a high pass (HP = high pass response, LP = low pass response) :

$$HP = 1 - LP$$

$$HP = 1 - \frac{1}{s^2 + 2s + 1}$$

$$HP = \frac{s^2 + 2s}{s^2 + 2s + 1}$$

This is not the same as a standard high pass transfer equation:

$$HP = \frac{s^2}{s^2 + 2s + 1}$$

Thus we get an asymmetrical transfer function that will meet the constant voltage requirement of the CPC but not the constant power requirement of the APC.

The second option is a slight variation on the first: cascading two state-variable filters. The first will be tuned for the lower crossover frequency and the second for the upper crossover frequency. State variable filters have both high pass and lowpass (as well as bandpass) outputs. The lowpass output of the first section will be the woofer signal. The highpass output of the first section will be the input of the second section. The second section's lowpass output will then be a bandpass output which will be our midrange signal. The highpass output will be the tweeter signal.

This approach has the advantage of having no possible “hole” in the frequency response due to misalignment of the filter response. Since the same frequency determining components determine both high and low pass responses for each section, the responses must be the same. The disadvantage to this approach is that the number of components is increased. The signal passes through more op amps in this configuration.

Next we look at the brute force approach of building the filters out of second-order sections. We shall build the bandpass section as a combination of lowpass and high pass sections, since the crossover frequencies are more than an octave apart. We will use Sallen-Key filters, since they are the least dependent on the op amp parameters (although at the frequencies at which we are working, this is probably not a major consideration).

We have chosen a second order APC, also known as a Linkwitz-Riley response. This response is a Butterworth squared response. Therefore, the damping ratio is 1. The lower crossover point is 319 Hz. and the upper is 5300 Hz, the same as in the passive implementation. The component calculations are given in Appendix II. The final schematic is Figure 8.88. Note that the inversion required for the midrange is not provided for in the crossover, and must be accomplished in the system

wiring. The measured frequency response of the active network is given in Figure 8.89.

It is advisable to insert a coupling capacitor between the power amplifier and the tweeter to protect it from turn on transients which can contain significant low frequency energy. These transients can easily turn the tweeter voice coil into an expensive fuse! The capacitor should be chosen so that it does not affect the transfer equation. Positioning the corner frequency a decade or greater below the upper crossover frequency is more than sufficient. Use a high quality film capacitor.

There are several other functions active crossovers can accomplish. The main one is to introduce time delays into the signal path. This allows the speakers to appear to have their acoustic centers aligned, even though they are mounted on a common baffle. This has an effect on the imaging characteristics of the system. The time delay can be implemented with *allpass* filters, which give a constant time delay (phase shift) and a flat amplitude response.

Subjective evaluations indicate active crossover networks sound better than their passive equivalents. Although they offer the ultimate in audio performance, the cost effectiveness of the active crossover must be determined by the designer.

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# CROSSOVER NETWORK: APPENDIX 1

## PASSIVE CROSSOVER CALCULATIONS

The following design equations are from Robert Bullock's *Passive Crossover Networks Part II*. The equations were entered into a spreadsheet to facilitate manipulation. The crossover frequencies were manipulated so that inductor values fell as close as possible to standard values.

DRIVER	PART NO.	IMPEDANCE	SENSITIVITY
WOOFER	MADISOUND 1252DVC	3.2Ω	90
MIDRANGE	AUDAX HD12P25FSM	6.5Ω	93.6
TWEETER	AUDAX HD100D25	7Ω	91.5
LOW CROSSOVER FREQ: 319 Hz	(FL)	W1 =	2*PI*FL
HIGH CROSSOVER FREQ: 5300 Hz	(FH)	W3 =	2*PI*FH
		FM =	SQRT(FL*FH)
		W2 =	2*PI*FM
FREQUENCY SPREAD	16.61442	(S =	FH/FL)
SQUARE ROOT OF S	4.076079	(R =	SQRT S)

The sensitivities of the drivers are rarely the same. This means that if we provide the same signal level to the drivers, their acoustic outputs would differ. The fact that we are using an unequal number of multiple drivers also affects the sensitivity. The excess gain calculation allows the level equalization. From this we get a pad resistor. The sum of the pad resistor and the equalized driver impedance is the load resistance for the design equations:

### EXCESS GAIN CALCULATIONS:

MINIMUM SENSITIVITY	=	90	(WOOFER)
TOTAL SENSITIVITY:	WOOFER =	90	
	MIDRANGE =	98.37121	
	TWEETER =	94.5103	
EXCESS GAIN:	MIDRANGE =	8.371 dB	(2.622)
	TWEETER =	4.510 dB	(1.681)
PAD RESISTORS:	MIDRANGE =	3.5Ω	(RM)
	TWEETER =	2.38Ω	(RT)
DESIGN IMPEDANCE:	WOOFER =	3.2Ω	
	MIDRANGE =	5.68Ω	
	TWEETER =	5.88Ω	

CROSSOVER CALCULATIONS:

FILTER SHAPE	a	=	$2(S-1)/(S^2-2S)$
		=	2.004114
GAIN PARAMETER	H	=	$S+a^2-4+(3/S)$
		=	16.81146
BP SHAPE A	A	=	$a*(R+1/R)$
		=	8.414262
BP SHAPE B	B	=	$S+A^2+(1/S)$
		=	20.69108

				ACTUAL VALUE
				=====
C11	=	$1/a/RL/W1$	=	77.79596 $\mu$ F
L12	=	$a/RL/W1$	=	31 $\mu$ F+40 $\mu$ F+4.7 $\mu$ F
L31	=	$a*RH/W3$	=	3.1996mH
C32	=	$1/a/RH/W3$	=	0.354mH
				0.35mH
				2.5 $\mu$ F
K	=	B-1	=	19.69108
E	=	$A(1-1/K)$	=	7.986948
RA	=	$RM(K/H-1)$	=	0.972933 $\Omega$
R0	=	RA+RM	=	4.486 $\Omega$
				4.5 $\Omega$
C21	=	$1/A/R0/W2$	=	2.186 $\mu$ F
L22	=	$A*R0/W2/K$	=	2.2 $\mu$ F
L23	=	$E*R0/W2$	=	0.3479mH
C24	=	$K/E/R0/W2$	=	0.354038mH
				0.35mH
				45 $\mu$ F

The design equations for the compensation network appear in Figures 8.76 and 8.77.

COMPENSATION COMPONENTS:

		CALCULATED		ACTUAL
		=====		=====
MIDRANGE:	RC	=	2.208 $\Omega$	2.2 $\Omega$
	CC	=	23.24 $\mu$ F	15 $\mu$ F+8 $\mu$ F
	RR	=	2.39 $\Omega$	2.4 $\Omega$
	LR	=	1.232mH	1.25mH
	CR	=	466.4 $\mu$ F	280 $\mu$ F+140 $\mu$ F+47 $\mu$ F
WOOFER:	RC	=	3.56 $\Omega$	3.3 $\Omega$
	CC	=	66.97 $\mu$ F	50 $\mu$ F+15 $\mu$ F+1 $\mu$ F

## SPEAKER CROSSOVERS: APPENDIX II

### ACTIVE CROSSOVER DESIGN

We will design the active crossover to have the same crossover frequencies as the passive crossover, namely 319 Hz. and 5300 Hz. We will also define the crossover as having the Linkwitz-Riely response which is a Butterworth squared response. Therefore the  $\alpha$  of the 2nd order section is 2. All sections are unity gain Sallen-Key as shown in Figure 8.86.

#### VOLTAGE CONTROLLED (LOWPASS) VOLTAGE SOURCE (SALLEN-KEY)

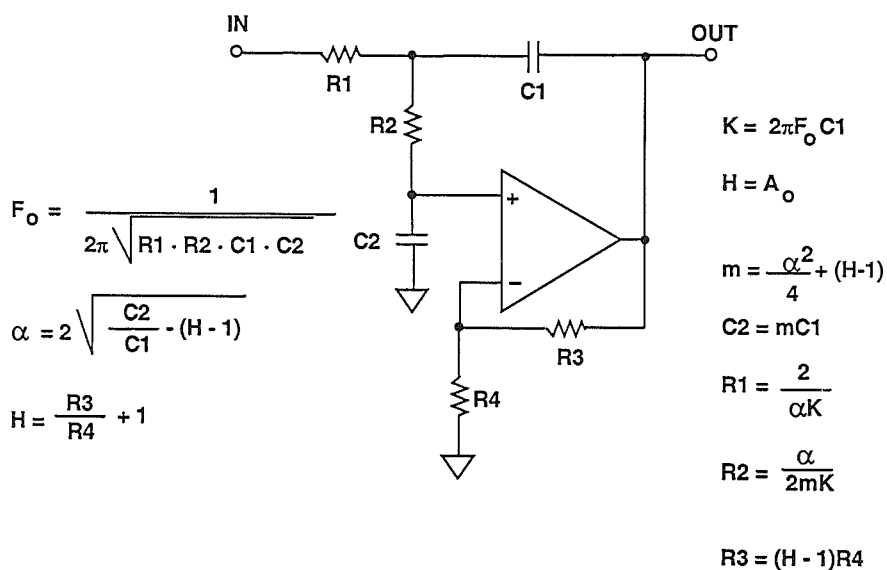


Figure 8.86

## LOWPASS DESIGN

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### SECTION 1, 319 Hz:

Choose	C1	=	0.1 $\mu$ F	
	k	=	$2 * \pi * F_0 * C1$	
		=	$200.4 \times 10^{-6}$	
	m	=	$\alpha^2 / 4 + (H - 1)$	
		=	1	
	C2	=	$m * C1$	
		=	0.1 $\mu$ F	
	R1	=	$2 / (\alpha * k)$	
		=	4.989k $\Omega$	use 4.99k $\Omega$
	R2	=	$\alpha / (2 * m * k)$	
		=	4.989k $\Omega$	use 4.99k $\Omega$

Since we cannot get the exact value required for the resistors and we don't particularly care what the exact crossover frequency is, we will calculate the exact frequency and use it for subsequent calculations.

$$F1 = \frac{1}{[2 * \pi * \text{SQRT}(R1 * R2 * C1 * C2)]}$$

$$= 319 \text{ Hz}$$

### SECTION 2, 5300 Hz:

Choose	C1	=	1000 pF	
	k	=	$33.30 \times 10^{-6}$	
	m	=	1	
	C2	=	1000 pF	
	R1	=	30.03k $\Omega$	use 30.1k $\Omega$
	R2	=	30.03k $\Omega$	use 30.1k $\Omega$

Again, we calculate the actual frequency value.

$$F2 = 5287 \text{ Hz.}$$

# HIGHPASS SECTIONS

## HIGHPASS SECTION (SALLEN-KEY)

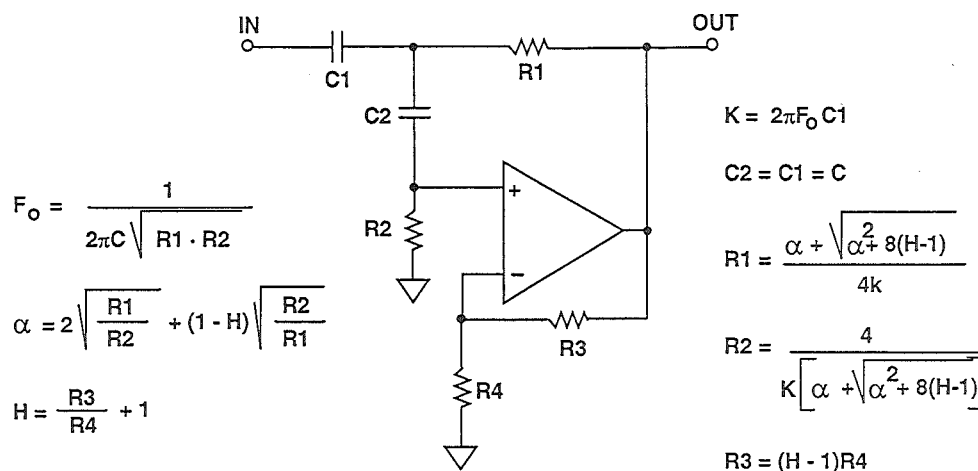


Figure 8.87

### SECTION 3, 319 Hz:

Choose	C	=	0.1μF	
	k	=	200 × 10 <sup>-6</sup>	
	m	=	1	
	R1	=	(1/4k)*[α+SQRT(α <sup>2</sup> +8(H-1))]	
		=	(1/4k)*[α+SQRT(α <sup>2</sup> )]	
		=	α/2k	
		=	4.989kΩ	use 4.99kΩ
	R2	=	(4/k)/[α+SQRT(α <sup>2</sup> +8(H-1))]	
		=	2/αk	
		=	4.989kΩ	use 4.99kΩ

### SECTION 4, 5270 Hz:

Choose	C	=	1000pF	
	k	=	33.11 × 10 <sup>-6</sup>	
	m	=	0.25	
	R1	=	15.1kΩ	use 15kΩ
	R2	=	60.4kΩ	



## ACTIVE CROSSOVER NETWORK

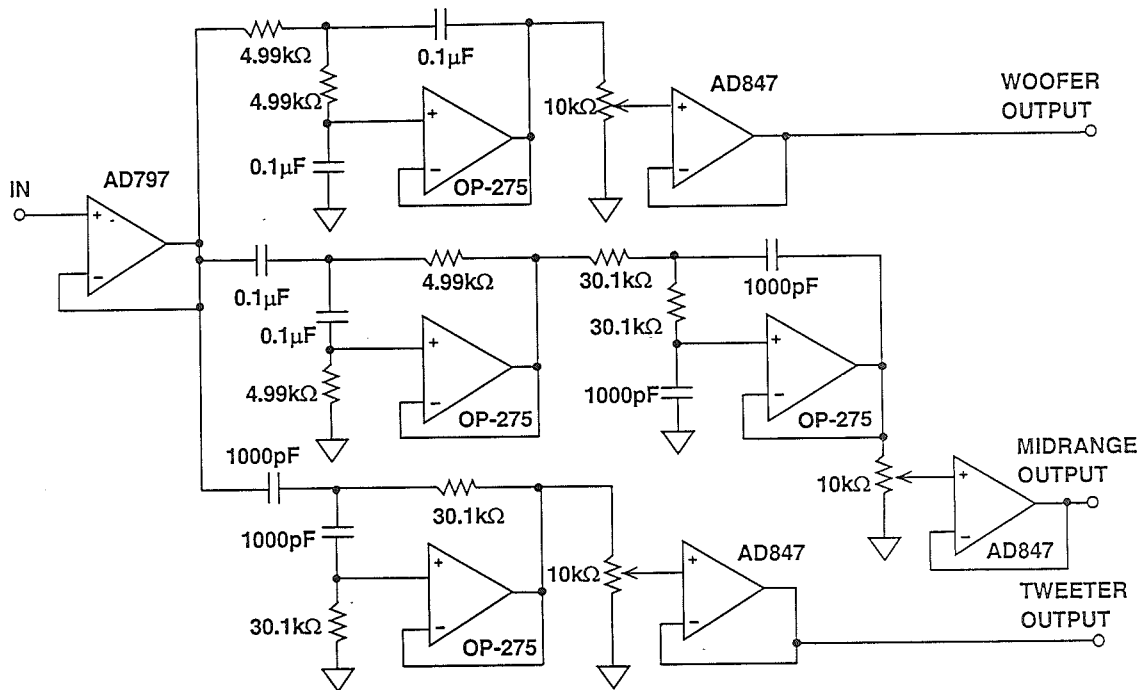


Figure 8.88

## ACTIVE CROSSOVER FREQUENCY RESPONSE

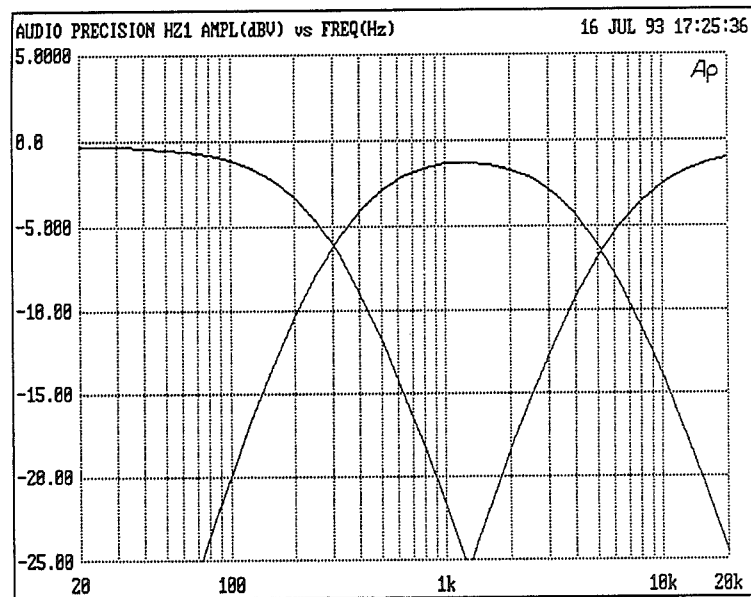


Figure 8.89



## DIGITAL AUDIO APPLICATIONS

### *Walt Kester*

Activities related to studio recording are complex and varied. Generally, many channels are used, with each dedicated to one or more signal sources (instruments/voices). All channels need not be recorded at the same time. Each channel is subjected to extensive processing such as gain control, filtering, non-linear compression or expansion, reverberation, spectral equalization, and other special-effects enhancements. The channels are then mixed together to obtain a final arrangement with the desired overall effect.

Traditionally, channel processing and mixing were implemented entirely in the analog domain—with numerous

disadvantages. Each channel's information—stored as an analog signal on magnetic tape—degrades as the cutting, splicing, and re-recording process progresses, undermining the benefits of the processing. The limited performance range available with analog processing sets a ceiling on the signal enhancement that can be obtained. Also, analog circuitry can only handle one channel at a time; multi-channel mixers are expensive and difficult to control. Finally, if analog processing hardware is used, overall mixing flexibility can be achieved only through hardware modifications. In practice, this means that the mixing process loses its ability to creatively explore special effects.

## DIGITAL AUDIO STUDIO TECHNIQUES

- Digital Recording: 16, 18 or 20 Bits for ADC
- Digital Mixing
- Gain Control
- Reverberation and Special Effects
- Equalization using Digital Filters

Figure 8.90

Increasingly, audio processing is relying on digital techniques to improve audio quality. The first step in this transition was digital recording, which became prevalent in the early 1980s. Audio signals are converted to digital form before being stored on magnetic tape. Digital recording eliminates several sources of degradation that affect analog recordings, including the effects of non-linearities and additive noise in the magnetic materials used for recording, and wow and flutter in the tape playback mechanism.

In studio mixing applications, however, digital recording does not eliminate all complications. In the mixing and enhancement process, information is passed from one tape to another—

requiring both ADCs and DACs, a source of noise. These conversions are no longer necessary if all processing and mixing are handled with DSP techniques.

In the DSP-based studio recording system shown in Figure 8.91, signals are digitized as early as possible, usually to 16, 18, or 20-bit resolution. After conversion, the audio processing is handled digitally with high performance DSP processors. Gain factors are handled with digital multiplication. Filtering and equalization can be handled with linear-phase FIR filters. Dynamic-range control is easily included in the system by using a multiplier for non-linear compression/expansion computations.

## DIGITAL AUDIO STUDIO SYSTEM

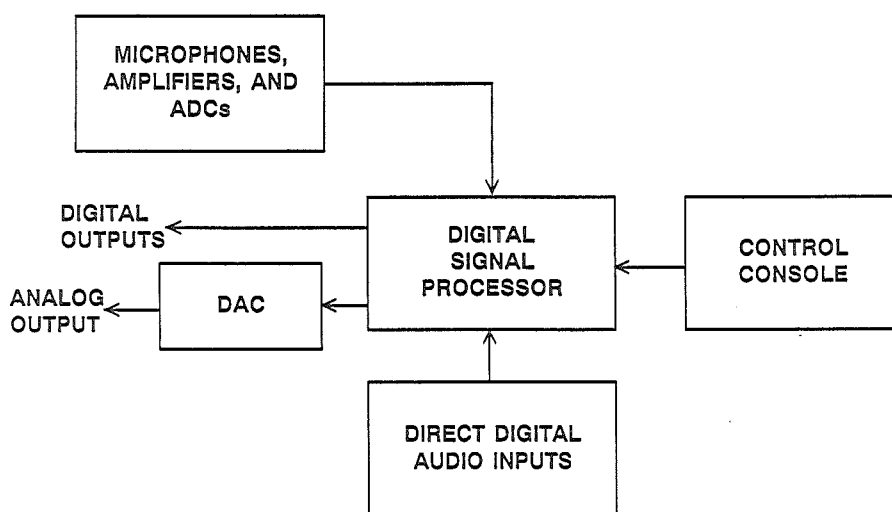


Figure 8.91

The traditional mixing process is also easily implemented with DSP. Digital channels to be mixed are simply added together. Delays can be introduced easily into channels, allowing phase delays to be equalized. Channel interconnections—which must be hardwired in an analog processor—can be reconfigured easily in a DSP system.

In addition to improving on traditional systems, a DSP studio recording system opens up numerous new options. Unusual special effects are readily included in the system. Reverberation effects can be modeled, simulated, and integrated into the final recording. Digital reverberation can give concert hall or cathedral ambience to what might have been recorded in a dry studio. An FFT routine's spectral analysis of the signal can form the basis for adaptive digital filters that provide optimal equalization.

With the advent of compact disc (CD) and digital audio tape (DAT) players, there is no requirement for digital-to-analog conversion anywhere in the studio recording process, except for monitoring. The final digital recording can be transferred directly to the CD or DAT in digital form with no loss in fidelity.

Although 18 and 20-bit ADCs may be used in the recording process, the standard for CD and DAT has been set at 16 bits. Additional bits may be used in the DSP studio processing to allow for roundoff errors, overflows, etc., but the final recording is truncated to 16 bits per sample on the CD or DAT. The sampling-rate standard for CD recordings is 44.1kSPS, and 48kSPS for DAT.

## DIGITAL AUDIO RECORDING STANDARDS

- 16-20 bits ADC Resolution, Truncated to 16 bits for Compact Disc
- 44.1kSPS Sampling Rate for CD Players
- 48kSPS Sampling Rate for Digital Audio Tape (DAT) Players

Figure 8.92

Performance of audio systems is primarily measured in terms of three dynamic specifications: Total harmonic distortion plus noise (THD+N), D-Range

distortion, and signal-to-noise ratio. These are defined in Figure 8.93.

## KEY AUDIO PERFORMANCE SPECIFICATIONS

- **THD + N:** Ratio of the Power of the Values of the Harmonics and Noise to the Power of the Fundamental Input Frequency Expressed in % or dB
- **D-Range Distortion:** Ratio of the Distortion Plus Noise to the Signal at a Signal Amplitude of -60dB FS. Add 60dB to the Ratio to Obtain D-Range Distortion Value
- **Signal-to-Noise Ratio:** Ratio of the Output Power with No Signal Present to the Output Power at Fullscale

**Figure 8.93**

## THE AD1879 18 BIT SIGMA-DELTA AUDIO ADC

The AD1879 is a dual 18 bit sigma-delta ADC designed to meet the stringent requirements of professional digital audio. A block diagram of the device is shown in Figure 8.94, and performance specifications are summarized in Figure 8.95. The input sigma-delta modulator is a fifth-order differential switched capacitor design which performs the quantization noise shaping function.

The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kSPS. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC. For less exacting applications, the AD1878 is a 16-bit version of the AD1879.

## AD1879 DUAL 18-BIT SIGMA-DELTA AUDIO ADC

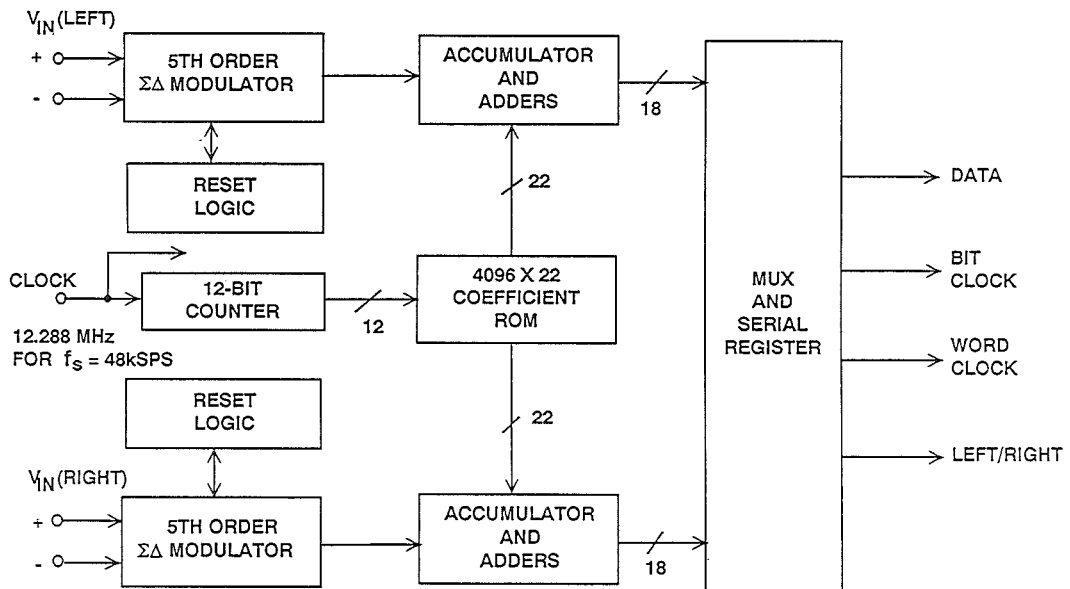


Figure 8.94

## AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- Two 18 Bit Channels for Stereo Digital Audio
- Interchannel Crosstalk: -110dB at 1kHz
- SNR: 104dB
- THD: 100dB
- Oversampling Ratio: 64x
- Output Word Rate: 55kHz Maximum
- Linear Phase Digital Filter
- Power: 900mW
- 28 Pin, 600-mil Plastic Package

Figure 8.95

For audio ADCs such as the AD1879, the digital lowpass filter cannot be implemented using standard multiply-accumulate structures because semiconductor technology is not yet fast enough. For example, we require a filter which operates at a sample rate of 3.072MHz (64 x 48kHz), is flat to 20kHz and has a stopband attenuation of over 115dB starting at 26.2kHz. If we enter these requirements into a standard FIR equiripple design program, the number of coefficients required turns out to be 4096. At an output

sample rate of 48kHz, we would require a multiply-accumulate time of 5.1ns. This is too fast for a standard FIR filter structure. Therefore we must use either a parallel processing approach where more than one multiply-accumulate is executed at any one time, or a multi-rate approach where the decimation is done in more than one step. For the AD1879, a parallel processing approach was chosen (Reference 1). The characteristics of this filter are given in Figure 8.96, and the amplitude response in Figure 8.97.

### **AD1879 DIGITAL FILTER CHARACTERISTICS**

- Stopband Attenuation: 118dB
- Passband Ripple:  $\pm 0.0008$ dB
- Cutoff Frequency (48kHz output rate): 21.7kHz
- Stopband Frequency (48kHz output rate): 26.2kHz
- Number of Parallel Accumulators: 64 27-bit accumulators
- Coefficient Wordlength: 22bits
- Number of Taps: 4096

**Figure 8.96**



## AD1879 DIGITAL FILTER RESPONSE

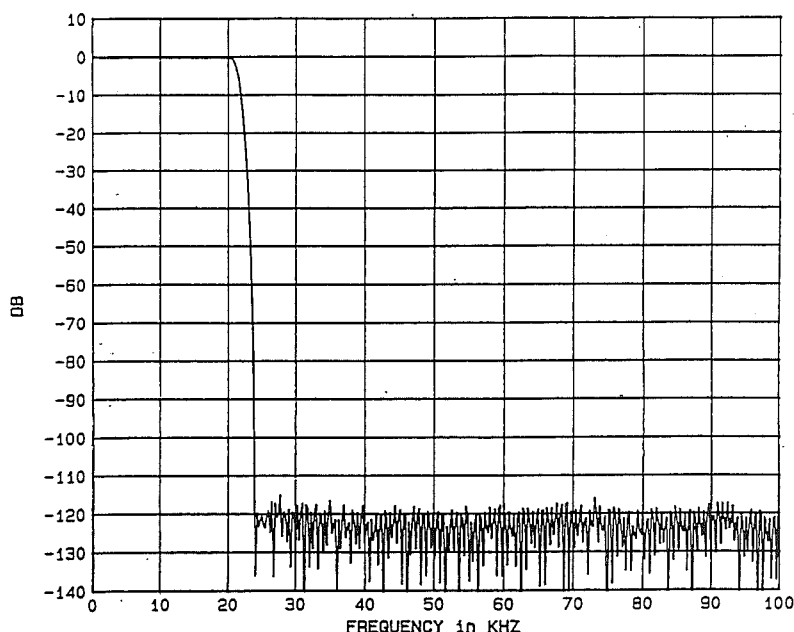


Figure 8.97

The AD1879 switched capacitor input circuit presents a special set of problems for the drive amplifier because of signal-dependent transient input currents. In order to understand the phenomenon better, Figure 8.98 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling rate,  $f_s$ , and acts as a resistor having a resistance equal to  $1/Cf_s$ . The integrator

time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 8.99. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier is signal dependent.

## SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

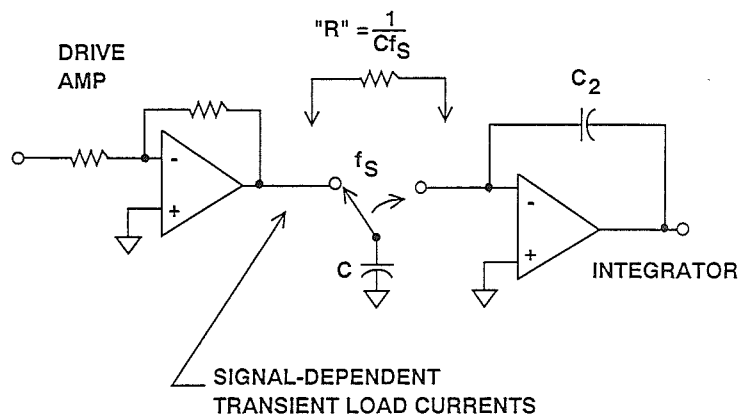


Figure 8.98

## CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

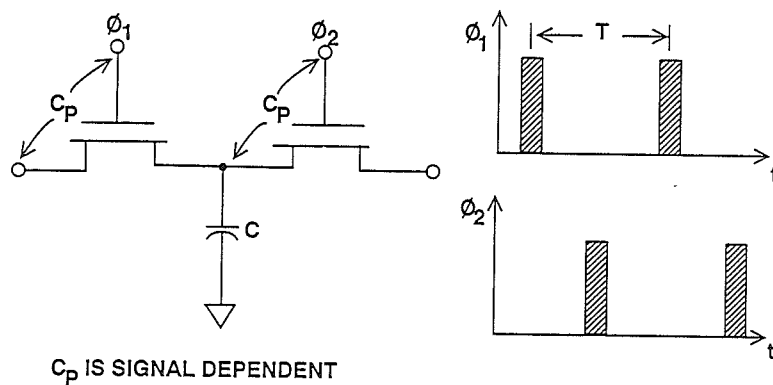


Figure 8.99

The sigma-delta modulator in the AD1879 is fully differential and has the equivalent input circuit shown in Figure 8.100 (only one input channel shown). For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected  $0.0047\mu\text{F}$  capacitor supplies most of the differential-mode transient currents, while the  $0.01\mu\text{F}$  capacitors connected to ground absorb spike currents which are com-

mon mode. The  $51\Omega$  series resistors isolate the remaining transient current from the drive amplifiers as well as isolate the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion because of the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as a suitable precision low-distortion drive amplifier.

### DIFFERENTIAL DRIVER (ONE CHANNEL) FOR AD1879 SIGMA-DELTA AUDIO ADC

8

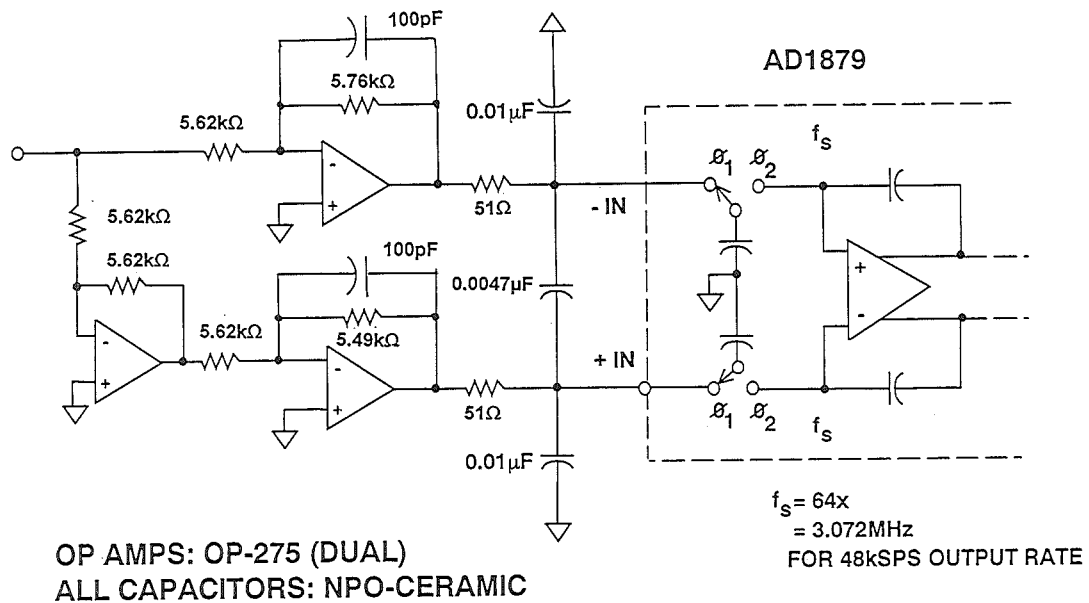


Figure 8.100

## APPLICATIONS FOR AUDIO DACs IN COMPACT DISC (CD) PLAYER ELECTRONICS

A simplified block diagram of the read electronics for a typical CD player is shown in Figure 8.101. The read electronics takes the data from the CD read head and performs the necessary data qualification, error detection and error correction. Data from the read electronics is in serial format, 16 bits per sample, at an effective sampling rate of

44.1kHz per channel. Data for the two channels is usually multiplexed in a single 1.4112MHz bit stream. In theory, it is possible to reconstruct the audio signal using two 16-bit DACs preceded by a digital demultiplexer and parallel-to-serial converters operating at an update rate of 44.1kHz followed by analog anti-imaging filters.

### COMPACT DISC PLAYER READ ELECTRONICS

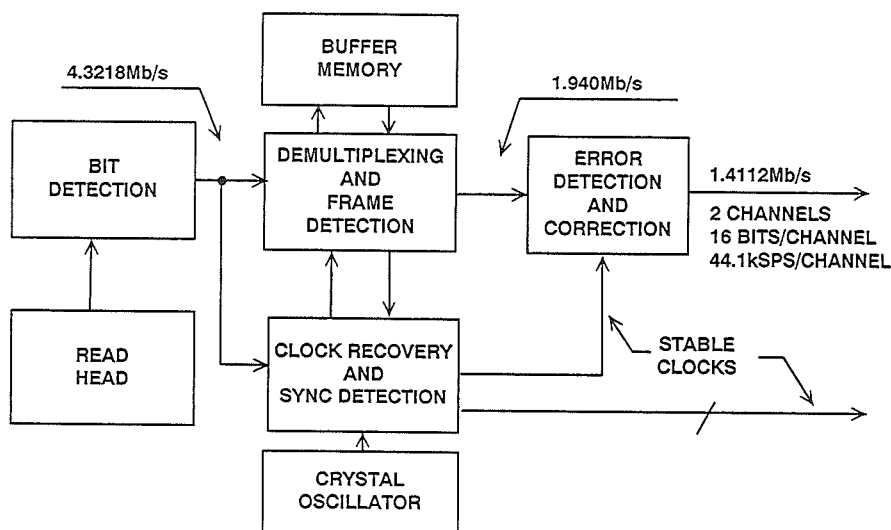


Figure 8.101

First-generation CD players used this approach as shown in Figure 8.102. An alternative is a single 16 bit DAC with output multiplexing for left and right channel. But sampling at 44.1kHz places severe requirements on the antialiasing filters. The audio bandwidth extends from 20Hz to 20,000Hz, and the filters must exhibit a flat frequency response over this frequency. In order to prevent aliasing, the filters must have at least 40dB to 50dB at-

tenuation at 22.05kHz which implies a complicated and costly 9- to 13-pole analog filter. Higher-order filters typically have non-linear phase response which is undesirable in audio applications. For this reason, the principles of oversampling and digital filtering are now in widespread use to simplify the design of the analog filter as well as increase the overall signal-to-noise ratio.

## FIRST-GENERATION CD PLAYER RECONSTRUCTION ELECTRONICS

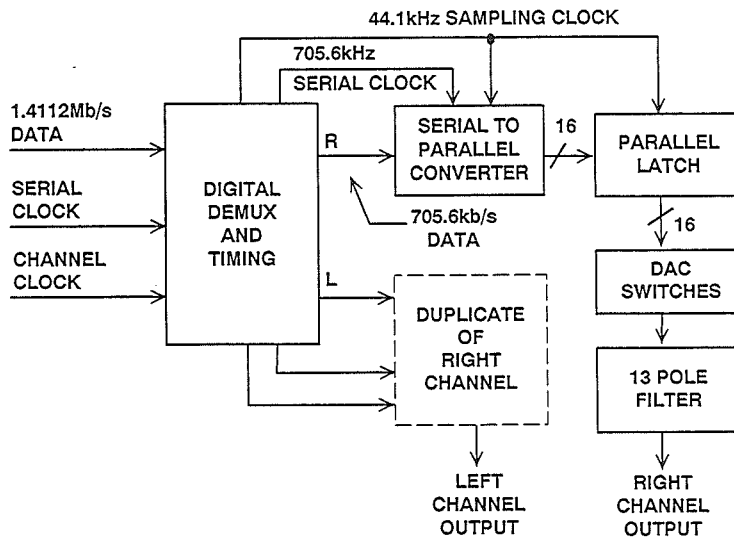


Figure 8.102

## 8X OVERSAMPLED 18-BIT CD PLAYER RECONSTRUCTION ELECTRONICS

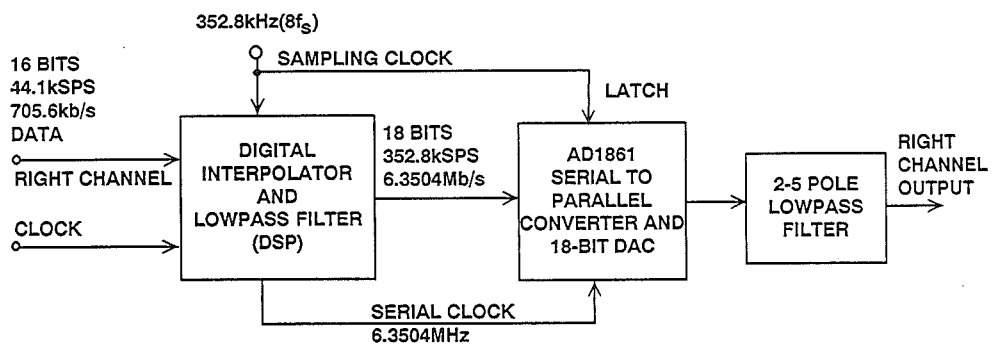


Figure 8.103

Second-generation CD players typically used oversampling ratios of 2x (88.2kSPS) or 4x(176.4kSPS) in conjunction with linear phase FIR digital interpolation filter chips. Third-generation players are using 8x oversampling (352.8kSPS) as shown in Figure 8.103, and the trend for future players will probably be 16x (705.6kSPS) or higher.

In addition to easing the requirements on the anti-imaging filter, oversampling followed by digital filtering spreads the quantization noise over a wider bandwidth, giving an improvement in SNR of  $10 \log_{10}(K)$ , where K is the oversampling ratio. This implies that for an oversampling ratio of 8x, there is

a theoretical 9dB (or 1.5bits) improvement in SNR. It is possible to carry the arithmetic in the digital interpolation filter out to 18 bits, drive an 18-bit audio DAC with the result, and realize this improvement in practical CD players. If 16x oversampling were used, the theoretical improvement in SNR would be 12dB, or 2 bits (Figure 8.104). A block diagram of a the complete reconstruction channel of an 8x oversampled 18 bit CD player is shown in Figure 8.105. The design is based on the dual 18 bit AD1865 DAC. Because of the 8x oversampling ratio, the output filter is a simple 3-pole filter (Figure 8.106).

### EFFECTS OF OVERSAMPLING AND DIGITAL FILTERING ON CD PLAYER DESIGN

Oversampling Ratio K	Theoretical Increase in SNR	Useful Bits of DAC Resolution	Number of Poles Required in Analog Filter
1	0dB	16	10
2	3dB	16	5
4	6dB	16/18	4
8	9dB	16/18/20	3
16	12dB	16/18/20	2

Figure 8.104

## 8X OVERSAMPLED CD PLAYER RECONSTRUCTION ELECTRONICS USING AD1865 DUAL 18-BIT AUDIO DAC

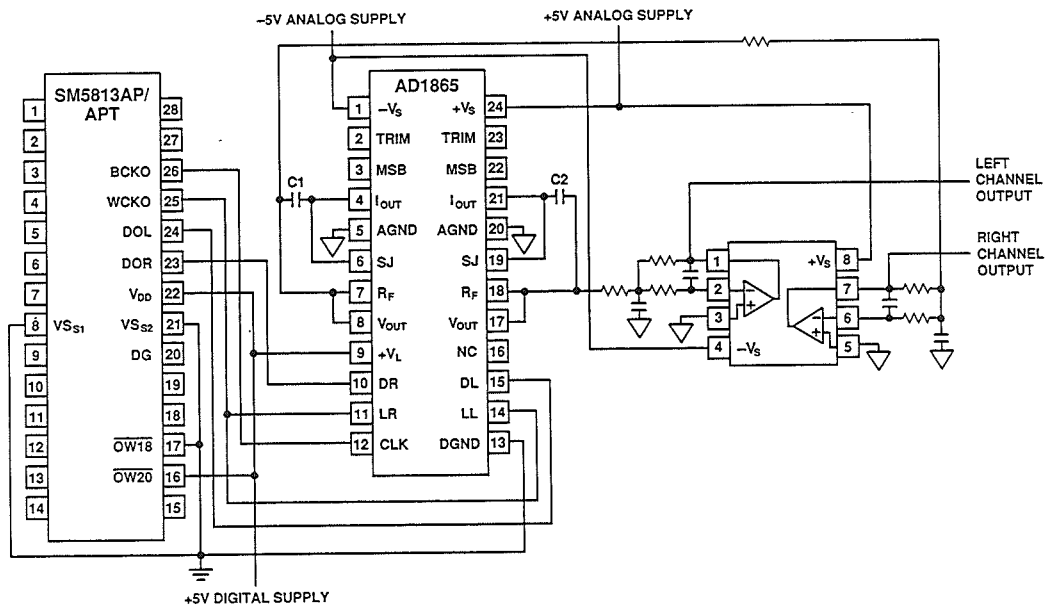


Figure 8.105

## 3-POLE ANTIALIASING FILTER FOR 18-BIT, 8X OVERSAMPLING

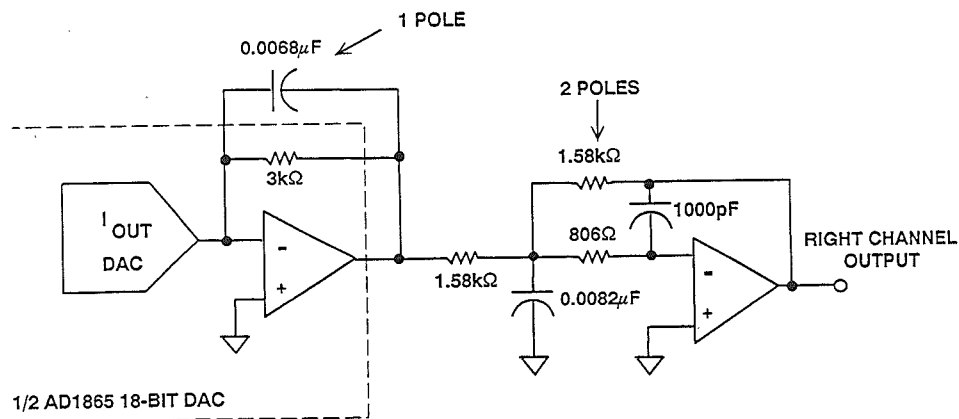
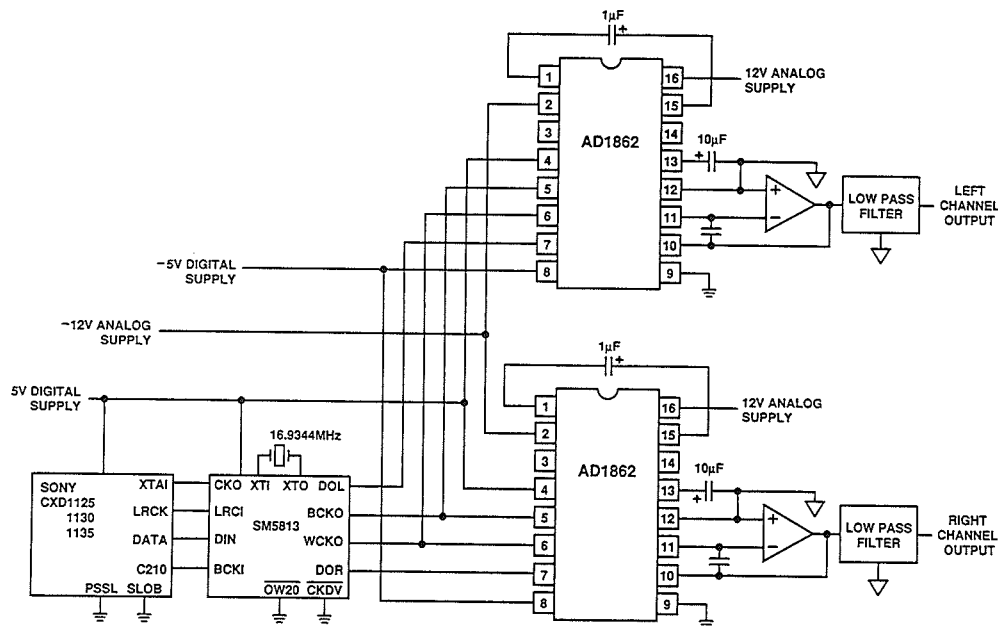


Figure 8.106

An additional reason for using DACs with greater than 16-bit resolution is that the process of digital interpolation and filtering adds truncation noise when the digital filter rounds off the interpolated values. This noise is reduced by using 18- and even 20-bit DACs to preserve accuracy in the interpolated values. A block diagram of a 20-bit, 8x oversampling CD filter and

DAC configuration is shown in Figure 8.107. Because of the 8x oversampling ratio, a 5-pole lowpass filter is sufficient to maintain the required performance. Typical THD + N performance for the system (including the output filter) is shown in Figure 8.108. A variety of CD digital interpolation filter chips are currently available from manufacturers such as Yamaha, NPC, and Sony.

# HIGH PERFORMANCE 20-BIT 8X OVERSAMPLING CD RECONSTRUCTION ELECTRONICS



**Figure 8.107**



## THD + N PERFORMANCE OF 20-BIT, 8X OVERSAMPLING CD ELECTRONICS USING THE AD1862 AUDIO DAC

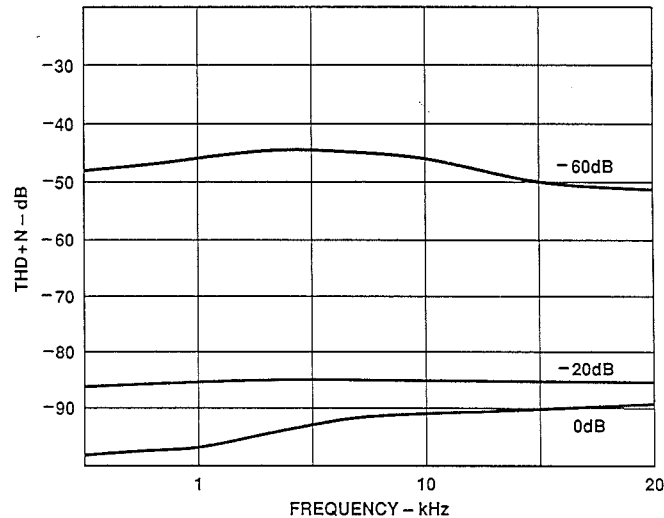


Figure 8.108

There are a number of audio DACs currently available on the market ranging from 16 to 20-bit resolution. Newer devices are capable of sampling rates up to 768kSPS, allowing 16x oversampling. Unlike traditional DACs, audio DACs are specified in terms of ac parameters such as THD + N, SNR, and D-Range Distortion because traditional dc specifications are not critical for audio applications. Audio DACs accept

serial inputs and have internal serial-to-parallel converters followed by a parallel latch. Two clock inputs are therefore required to operate an audio DAC. A serial clock is needed to strobe the serial data into the serial-to-parallel converter, and a latch-enable clock is required to strobe the parallel latch. A simplified block diagram of a typical digital audio DAC is shown in Figure 8.109.

## TYPICAL CD AUDIO DAC (SINGLE CHANNEL, 18 BITS, 8X OVERSAMPLING)

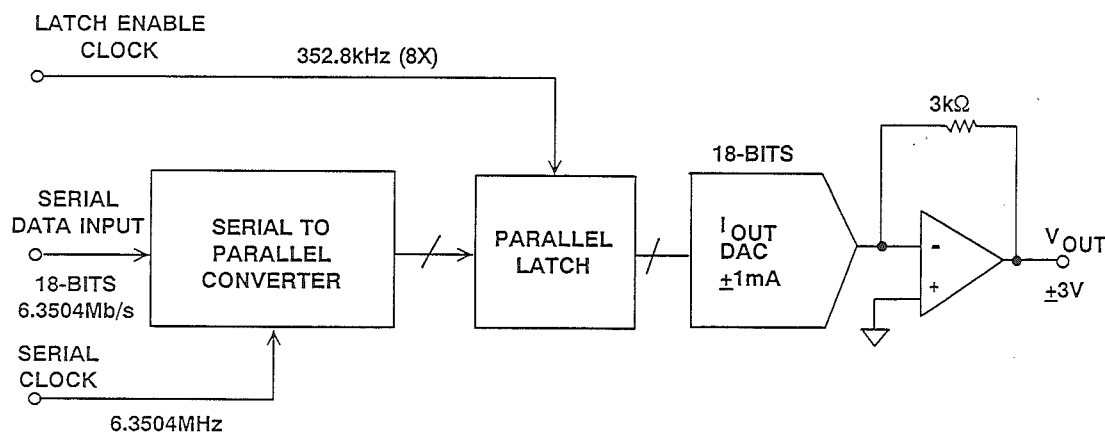


Figure 8.109

## DAC ARCHITECTURES

CMOS DACs for audio applications are often based on the current-mode steering circuit shown in Figure 8.110. An external reference is applied to the  $V_{\text{ref}}$  pin, and the R-2R ladder divides the input current  $I$  into binary-weighted currents as shown. The output drives the virtual ground of an inverting op amp. The finite “on” resistance of the FET switches is compensated for by placing an equivalent compensating FET in series with the feedback resistor  $R$ .

For high-performance DACs in the voiceband and audio range, BiMOS

processes (bipolar and CMOS devices on the same process) offer the advantages of low-power CMOS for the digital circuits (such as parallel-to-serial converters and latches) along with the low-glitch fast-switching performance of bipolar transistors. A typical current switch cell for such a DAC (the AD1861 18-bit audio DAC) is shown in Figure 8.111. The outputs of CMOS latches are level shifted by the two FETs and converted into a low-level  $\pm 0.8\text{V}$  differential drive for the NPN differential pair.

## CURRENT-STEERING CMOS DAC

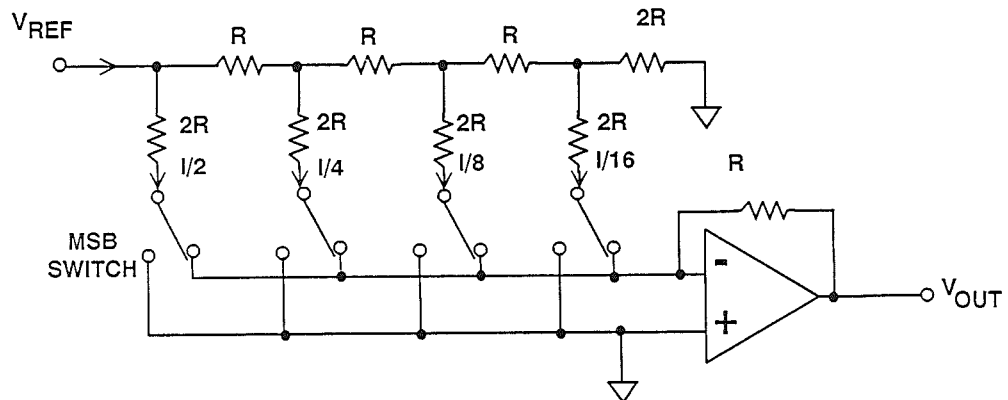


Figure 8.110

## BiMOS CURRENT SWITCH

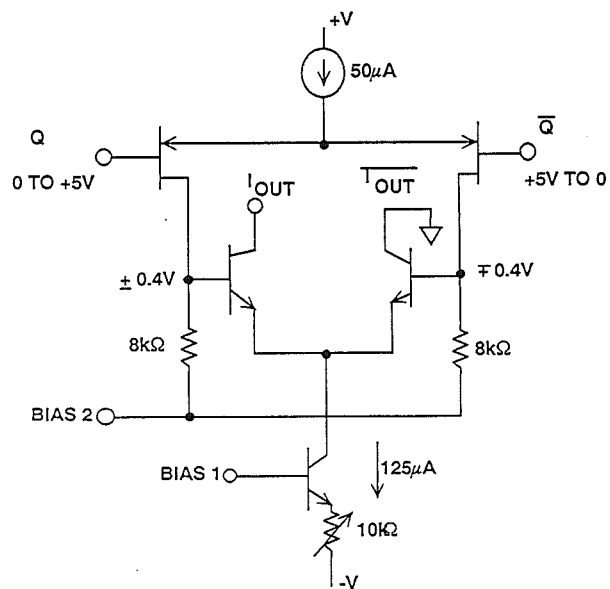


Figure 8.111

## GLITCH REDUCTION BY SEGMENTATION

If real estate, cost, power, and capacitance were of no consideration, the ideal “glitchless” DAC would consist of  $2^N - 1$  equally weighted current switches preceded by latches and decoding logic as shown in Figure 8.112. The glitch produced by switching between levels is

code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves.

## IDEAL DAC FOR MINIMUM SIGNAL-DEPENDENT GLITCH

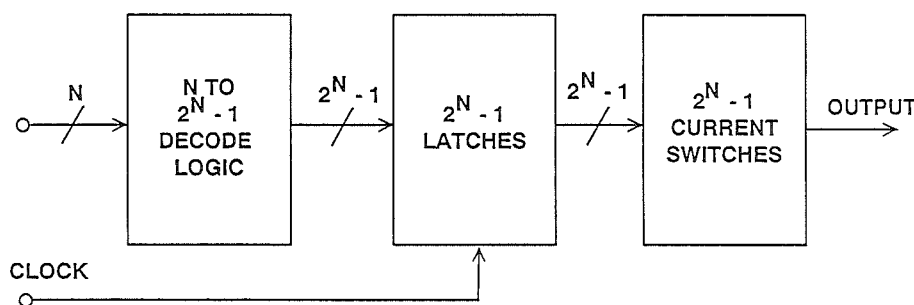


Figure 8.112

The scheme shown in Figure 8.112 is obviously not practical for high resolution DACs, but a significant amount of glitch reduction can be achieved by applying the concept to the first few MSBs. A block diagram of the segmentation technique used in the AD1861 18 bit audio DAC is shown in Figure 8.113. The AD1861 uses a combination of segmentation and R-2R division to achieve excellent linearity and low distortion. The four MSBs are decoded into a 15 bit “thermometer” code after the serial-to-parallel conversion. The 15 decoded lines (representing the 4 MSBs)

and the 14 LSB lines are then fed to a 29 bit latch. The 15 thermometer decoded lines each drive current switches having equal weights. The 14 LSB lines drive a conventional binary-weighted R-2R DAC. This combination of segmentation and conventional R-2R architecture along with laser trimmed thin film resistors allows the AD1861 to meet stringent audio specifications without the need for an external SHA deglitcher. A summary of key performance specifications for the AD1861 is given in Figure 8.114.

## SEGMENTATION IN THE AD1861 18-BIT AUDIO DAC

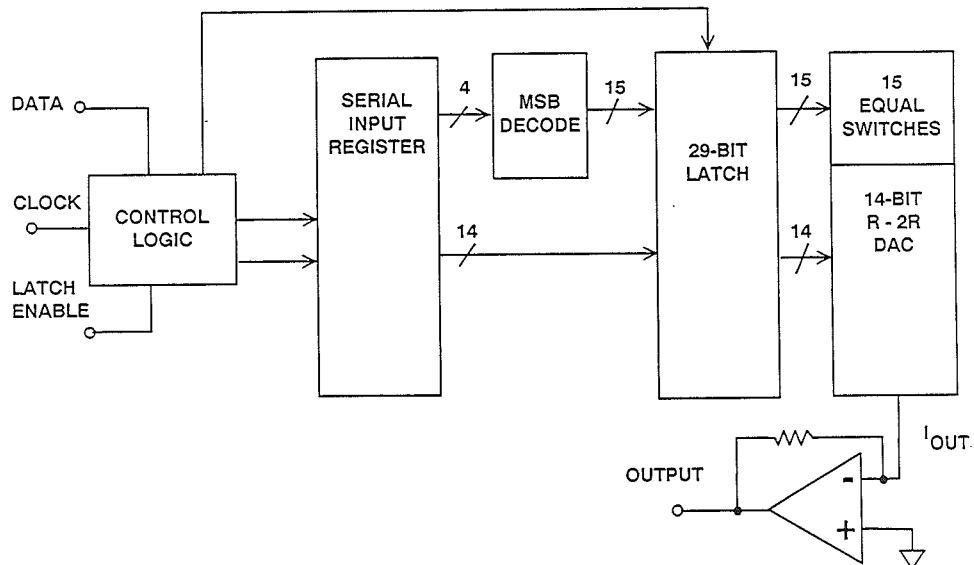


Figure 8.113

## AD1861 18-BIT AUDIO DAC KEY SPECIFICATIONS

- 108dB SNR
- 0.002% THD + N @ 0dB Signal Amplitude
- Up to 16x Oversampling Capability (768kSPS)
- $\pm 3V$  or  $\pm 1mA$  Output Capability
- 110mW Power Dissipation
- 16 Pin DIP Package

Figure 8.114

## AUDIO DAC GLITCH REDUCTION USING DIGITAL OFFSET

Regardless of the architecture used to design a high performance DAC, the most troublesome code-dependent glitch typically occurs at the midscale code transition, i.e. from 0111...1 to 1000...0. In an audio system which operates with bipolar signals, the midscale glitch noise is particularly troublesome, since it can introduce distortion for very low-

level passages. If a small digital offset is added to the DAC input, then the DAC midscale glitch noise will only occur at slightly higher input signals where it is less objectionable. Unfortunately, one end of the DACs range will be clipped by an amount equal to the injected digital offset (Figure 8.115).

### DAC WITH 1 / 16 FULLSCALE DIGITAL OFFSET

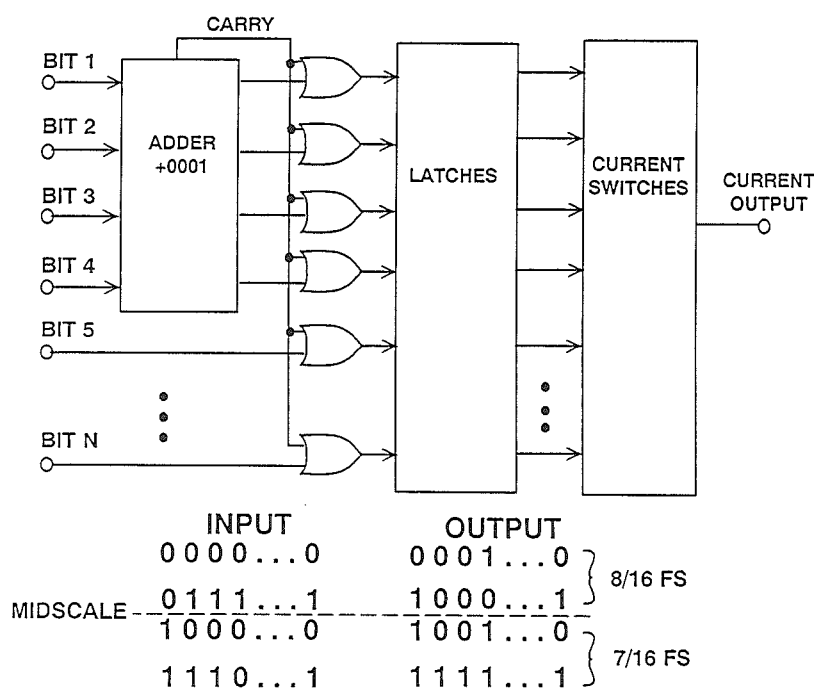


Figure 8.115

The AD1862 20 bit digital audio DAC uses a combination of segmentation and digital offset to achieve a high level of performance. The novel architecture prevents clipping and allows the full range of the 20 bit DAC to be utilized. A block diagram of the AD1862 is shown in Figure 8.116. The digital offset is accomplished by adding 0001 (1/16th

fullscale) to the four MSBs. The three MSBs are then segmented into a 7 bit thermometer code output which is latched and then drives seven equal current switches. Bit 4 (after the addition), and bits 5 through 20 are latched and then drive a conventional R-2R DAC. In order to prevent clipping at the positive end of the range, the carry

output of the adder drives an additional current switch having a weight corresponding to bit 4. Finally, an offset current equal to 1/16th fullscale is subtracted from the DAC output to compensate for the constant digital

offset. This architecture results in exceptional THD + N performance as shown in Figure 8.117. Key specifications for the AD1862 are summarized in Figure 8.118.

### AD1862 20-BIT AUDIO DAC USES DIGITAL OFFSET AND SEGMENTATION

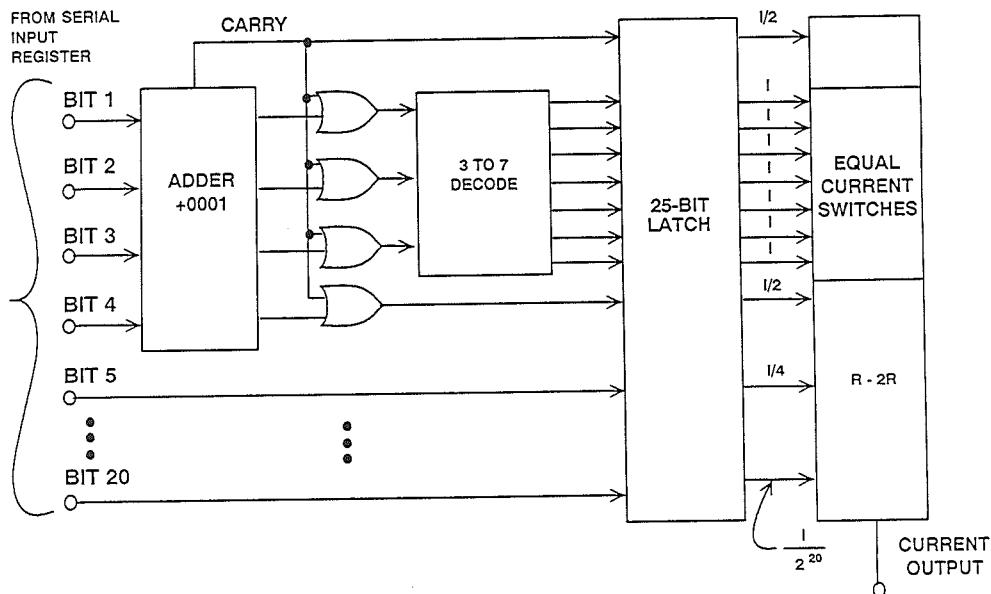


Figure 8.116

## THD + N VERSUS INPUT FREQUENCY FOR AD1862 20-BIT AUDIO DAC

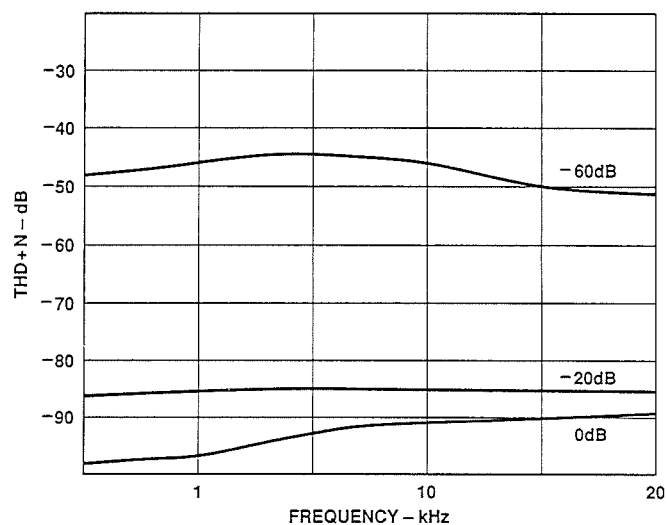


Figure 8.117

## AD1862 20-BIT AUDIO DAC KEY SPECIFICATIONS

- 119dB SNR
- 0.0012% THD + N @ 0dB Signal Amplitude
- 16× Oversampling Capability (705.6kSPS)
- ±1dB Gain Linearity @ -90dB Amplitude
- ±1mA Output Current
- 288mW Power Dissipation
- 16 Pin DIP Package

Figure 8.118



## STEREO CODECS FOR MULTIMEDIA AND BUSINESS AUDIO APPLICATIONS

### *David Fair*

The AD1848 and AD1849 16-bit SoundPort® Stereo Codecs (coder/decoder) bring “audio system on a chip” integration to computer applications for multimedia sound and business audio. Operating from a single +5V supply, they allow sophisticated digital audio functions to be incorporated on PC or workstation motherboards or add-in boards easily and at low cost.

Both codecs include a stereo sigma-delta ADC and DAC, with their 1-bit, high-sampling-rate analog interface. They achieve a dynamic range of 80dB with total harmonic distortion plus noise of -74dB over the 0-to-20kHz audio band. They are fabricated in a digital CMOS process enhanced with a second layer of polysilicon to facilitate high-performance capacitor formation.

These codecs offer far more than just two pairs of integrated converters. On-chip oscillators provide for software selection of all the key multimedia sample rates from 5,500 samples/second to 48kSPS, via software selection of one of two external crystals and the appropriate division ratio; an external clock may also be supplied. Signal filters are provided on-chip to simplify design and reduce expense and space requirements. The sigma-delta a/d converters incorporate their own digital decimation filters

with maximum  $\pm 0.1$ -dB passband ripple. The d/a converters are preceded by an integral interpolation filter in the digital domain and followed by switched-capacitor and continuous-time analog filters to remove Nyquist images. No external references are required; they are included on the SoundPort codec chips.

In addition, both devices allow independent control of left- and right-channel input gain in 1.5dB steps, from 0 to +22.5dB. Microphone inputs have access to an additional +20dB gain block. Left- and right-channel outputs can be attenuated from 0 dB to -94.5dB, in 1.5dB steps, or muted (shut off) entirely. Both codecs support mixing of the a/d converter's output with the d/a converter's input for audio overlay (“karaoke” operation) under software control. The devices support pulse-code-modulated (PCM) 16-bit linear, 8-bit companded  $\mu$ -law, and 8-bit companded A-law data formats.

The AD1848 and AD1849 SoundPort codecs are basically similar; they differ principally in their digital interface. The AD1848 (Figure 8.119) has a byte-wide *parallel* data/control port that supports a buffered direct connection to the Industry Standard Architecture (ISA) or “PC-AT” bus. This AD1848 was

specified in a joint agreement between Analog Devices, Inc., Compaq Computer Corp., and Microsoft. Its objective was to provide the lowest cost and

simplest implementation of digital audio capabilities in an ISA-bus system. Key specifications for the AD1848 and AD1849 are shown in Figure 8.120.

## AD1848 PARALLEL-PORT 16-BIT SoundPort® STEREO CODEC

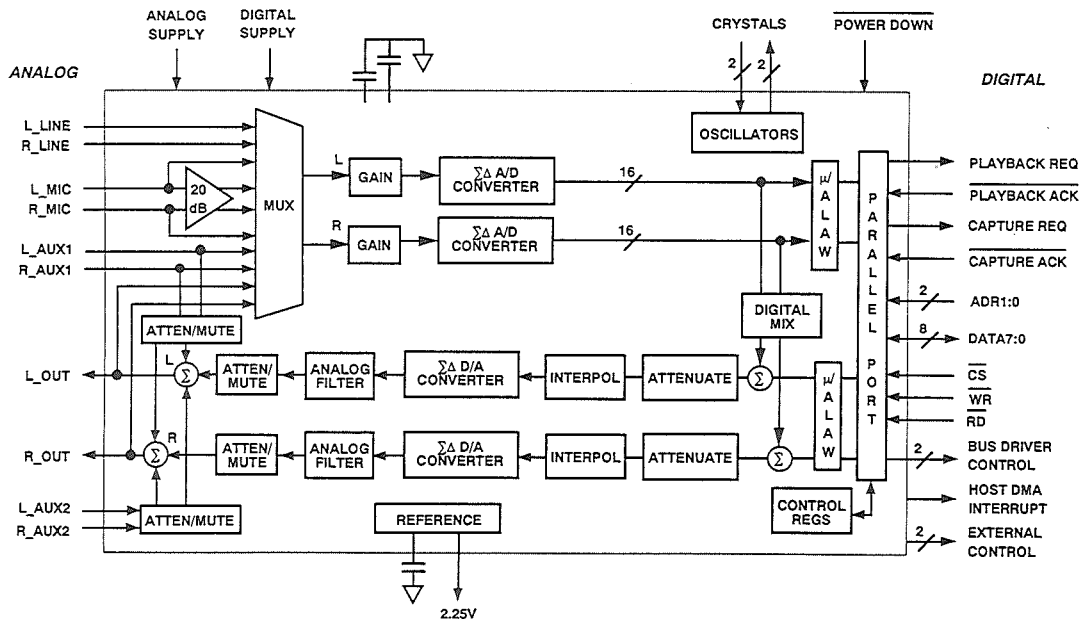


Figure 8.119

## AD1848/AD1849 AUDIO CODEC KEY FEATURES

- Single-Chip Integrated Sigma-Delta "Audio System-on-a-Chip"
- Dynamic Range of 80dB, THD + N of -74dB
- 5.5kHz to 48kHz Sampling Rates
- On-chip Signal Filters:
  - ◆ Digital decimation and interpolation
  - ◆ Analog output lowpass anti-imaging
- Programmable Gain and Attenuation
- 16-bit PCM linear or  $\mu$ -law / A-law companded data
- On-chip voltage reference and oscillators
- Operation from single +5V supply

Figure 8.120

Compaq uses the AD1848 in the newly announced DESKPRO® computers, and Microsoft uses it in their Windows Sound System® board. Since the precision AD1848 audio system cannot be expected to drive the capacitance of the

ISA bus directly, the interface uses an external '245-type digital bus transceiver for current buffering—but under control of the AD1848; it provides the Enable and Direction signals for the transceiver (Figure 8.121).

## INTERFACING THE AD1848 CODEC TO THE ISA COMPUTER BUS

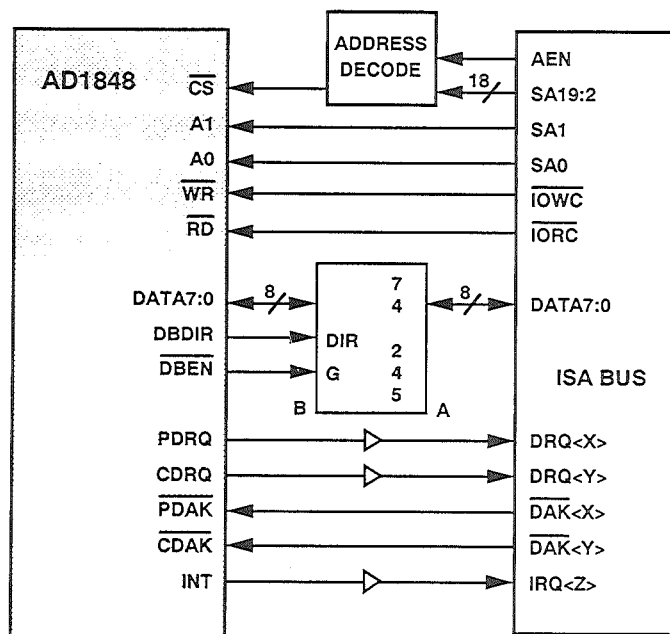


Figure 8.121

In contrast, the AD1849 (Figure 8.122) uses a *serial* interface for data and control information. This SoundPort was developed to meet the needs of Sun Microsystems Corporation's SPARCstation 10 series of UNIX workstations. Sun's original requirement for the serial interface was that it connect with the ISDN bus employed in these

new SPARCstations using minimal translation logic. Fortunately, the serial interface is general enough to allow direct or very simple connection to the serial ports of digital signal processors, including popular members of the ADSP-2100 family—as well as DSPs from other vendors as shown in Figure 8.123.

## AD1849 SERIAL-PORT 16-BIT SoundPort® STEREO CODEC

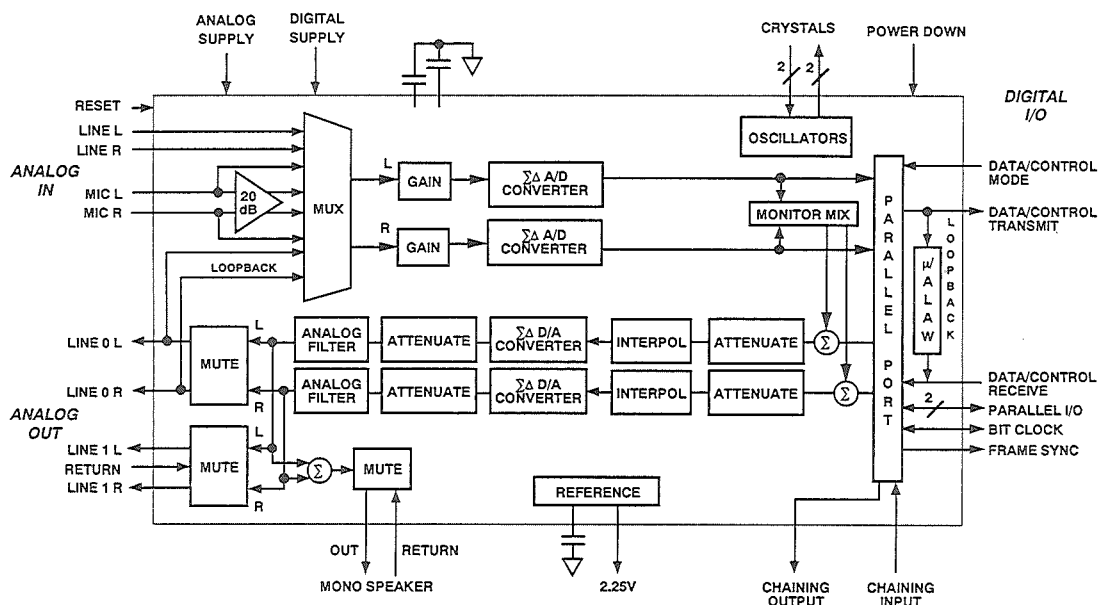


Figure 8.122

## AD1849 SERIAL CODEC DSP INTERFACE

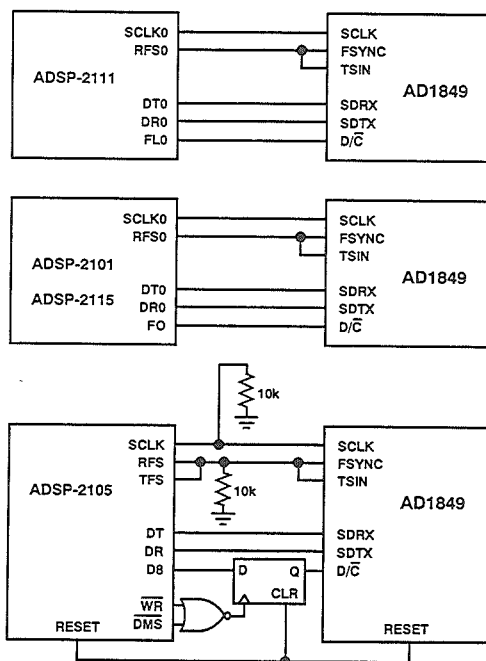


Figure 8.123

The direct connection to DSPs makes it possible to design very cost-effective digital audio “signal-computing” solutions (*Analog Dialogue* 26-2). The DSP can implement a wide range of compression/decompression and audio effects algorithms (such as filtering or equalization) using programs that can be either ROM-resident or downloaded from disk into local RAM.

Additional features of—and differences between—the AD1848 and AD1849 make available solutions for a variety of user needs. For example, the AD1848 parallel-port codec supports both programmed I/O (PIO) and direct memory access (DMA) transfers. In PIO, control information is transferred using the Read and Write strobes. Five registers are directly addressed via the two address pins of the IC. Two of these, used for address and data, indirectly access 16 additional byte-wide control registers, minimizing the number of PLCC package pins (68). Either one or two channels of DMA are supported via the Request and Acknowledge controls. A loadable, 16-bit DMA down-counter generates an external/internal interrupt on underflow.

For multimedia PC (MPC) compatibility, the AD1848 also has two stereo pairs of auxiliary line-level *analog*

inputs. Both channels can be independently mixed with the stereo DAC output in the analog domain. As the block diagram shows, this post-mixed analog signal is itself available as an input to the stereo a/d converters. The AD1848 also supports the MPC standard’s 8-bit unsigned data format at input and output.

The AD1849 serial-port codec has its own share of unique features. It will accept one of three clock sources: an external crystal, an external clock, or the serial port’s bit clock. The serial bus can support up to four devices via time-division multiplexing (TDM). It also has chaining inputs and outputs for sequential word synchronization when one, two, or four devices are “daisy-chained” on a single serial bus. Though more limited than the AD1848 with respect to analog inputs, the AD1849 offers an additional line-level stereo output driven from the stereo d/a converters, and an additional output for a monophonic speaker. The AD1849 is packaged in a 48-lead PLCC.

These two SoundPort codecs provide complete solutions for computer digital-audio applications requiring either parallel or serial interfacing. Though differing in detail, their capabilities are comparable overall.

## **SIGNAL COMPUTING AUDIO CHIPSETS AND ALGORITHMS**

Signal Computing is a technology framework and business model which recognizes that DSP-based signal-processing applications can benefit substantially by combining sets of high-performance processor- and interface chips with powerful, sophisticated algorithms from independent third parties (Independent Algorithm Vendors, or IAVs). Employing open designs and architectures, signal computing is characterized by well-defined levels of standardization that carefully define the hardware and software roles and the layers that make them up. This allows companies—both chip- and software vendors and OEM and system designers—to participate at the level where each brings maximum “value-added” expertise to the application. The chip supplier furnishes standard high-performance, low-cost ICs; the market-oriented algorithm developer provides the standard configurable software that produces the desired electronic perfor-

mance from the chips; and the OEM designer integrates them into a system specialized to meet the performance needed within his market niche. This environment avoids saddling the designer with the job of recreating all aspects of the overall design.

Low-cost digital signal processing is an “enabling” function, allowing broad expansion of *real-time* signal processing, through the combination of software and hardware defined as “signal computing.” Signal computing is characterized by the synchronized execution of algorithms on *real-time* data streams. It is quite distinct from the use of DSP, or any processor, in conventional numerical acceleration, where computations and graphics are simply speeded up—but still occur off-line: images are redrawn “more quickly” on the graphics workstation screen, but even though waiting time is reduced, it is still palpable.

## **PERSONAL SOUND SYSTEMS USING THE AD20MSP614 AUDIO CHIPSET**

The AD20msp614 Audio Chipset is the enabling chipset for Personal Sound System products. The AD20msp614 includes an ADSP-2115KP, AD1848KP, and ESC614. The ESC614 is a gate

array designed by Echo Speech Corporation which provides a PC to DSP interface. The personal sound system architecture is illustrated in Figure 8.125.

## SIGNAL COMPUTING: A TECHNOLOGY AND BUSINESS MODEL FOR REALTIME SIGNAL PROCESSING SOLUTIONS

- **Hardware Chipsets:**

Analog I/O (Codecs), DSP Processors, ASIC Interface Chips

- **Software Algorithms: Independent Algorithm Vendors (IAVs)**

- **Manufacturing Design Kits**

- **Typical Applications:**

Modems, Speech Processing, Music Processing, Digital Mobile Radio, Image Processing, Multimedia

8

Figure 8.124

### PERSONAL SOUND SYSTEM ARCHITECTURE

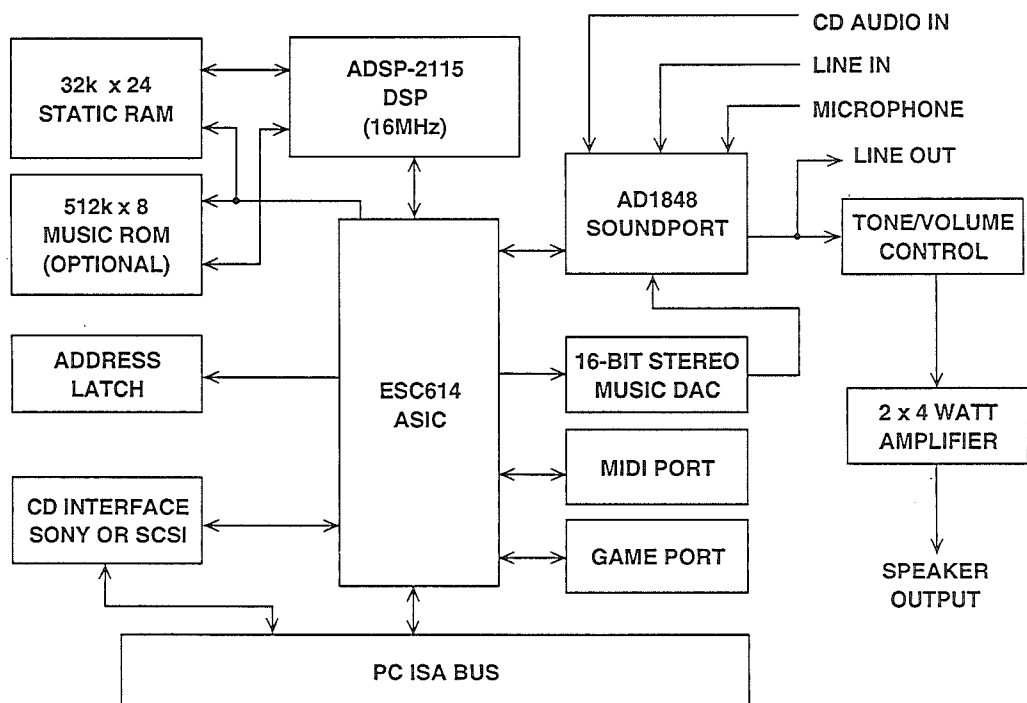


Figure 8.125

The ADMK-610 is a manufacturing kit which allows add-in card OEMs to enter the sound card market with a Personal Sound System product. The kit provides all an OEM needs to manufacture a Personal Sound System which supports Sound Blaster and Windows Sound System applications. The kit includes manufacturing information such as schematics, board layout, and parts lists. DSP algorithm software is included which provides Sound Blaster compatibility. Drivers for WAVE I/O, Musical Instrument Digital Interface (MIDI) MPU-401, and auxiliary functions (mixing, volume, and tone control) are also included in the kit. To complete the solution, Voyetra Multimedia Software, First Byte Monologue text-to-speech, and AudioFile audio application software are also included with the kits. Purchase of separate licenses from the respective software vendors is required

for all application software included in the kit. Purchase of the a EuSynth-1 music synthesis license from Analog Devices (ADLU-EUP02/-Q) is required for Sound Blaster compatibility.

Future upgrades to the ADMK-610 will enable Personal Sound System products to be upgraded to future capabilities such as EuSynth-2 wavetable music synthesis and speech and music compression.

The requirement for data compression represents a typical application for signal computing. Figure 8.126 shows the amount of hard disc storage required for various types of data. Notice that 72 minutes of digitized CD-quality audio requires approximately 700MB of storage. This would be impractical in multimedia applications without some type of data compression.

## THE NEED FOR DSP DATA COMPRESSION

■ 600 Pages of Text :	1MB
■ 20 Fax-Quality Images :	1.28MB
■ 5 Minutes of Digitized Voice :	2.4MB
■ 10 Color or Detailed Images :	75MB
■ 1 Minute of 1/4 Screen Animation :	147MB
■ 72 Minutes of Digitized CD Audio :	700MB
■ DSP Compression Algorithms are Available Which Can Reduce the Above by 6 : 1	

**Figure 8.126**



Various data compression algorithms have been written which can reduce this storage requirement by a factor of 5 to 6. The Dolby AC-2 Toolkit (ADLU-EUP01) is a software toolkit available from Dolby Labs. It includes software developed by EuPhonics which implements the Dolby AC-2 Audio compres-

sion/decompression algorithms on the ADSP21XX DSP processor. This algorithm achieves 5.6:1 compression of CD quality audio. It compresses 2 channels of 16-bit audio sampled at 44.1kHz. Both compression and decompression can be done on the ADSP-21XX in real time.

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